LTCC Dynamic Design Library (DDL)

One of the major projects in Prof. Wu’s group is the development of an advanced Dynamic Design Library (DDL) for LTCC circuit design.

This is the first software in the world that aims at a quasi-automatic LTCC circuit design. The objective of this project is to standardize the LTCC design procedure that will lead to higher unification of design solution.

Two proprietary techniques developed in the group are embedded in this software. One is a quasi-method of moment EM simulation engine tailored for LTCC circuit design. The software can accommodate effectively the effect of finite conductor thickness, which is a very critical issue in LTCC circuit design and irregular geometries. It has been demonstrated that the EM simulation engine is 100 to 500 times faster than commercially available EM simulation software.

Another unique technique used in DDL is the feature that the software can derive a physically expressive equivalent circuit model for a given accuracy and specified frequency range. With this feature, people can accurately assess the parasitics of embedded passives and diagnose where the unwanted parasitics happens in a quantitative way. Since the EM simulation engine is so fast, the design library derive the circuit model for a given geometry and physical dimension in real time.

The macro language used in DDL is fully compatible to that used in Ansoft HFSS version 8. Users have full freedom to define their own passive library and exchange the library component among users although the library will comes with a large number of component classes including various capacitors, inductors and filters.

A new design scheme called Dynamic Space Mapping Design Procedure is also developed in the group by using the DDL. With a full commitment on the development of the DDL, it is believed that the design cycle for LTCC circuit will be greatly reduced.