ITM1010
Computer and Communication Technologies

Lecture #7

Part I: Introduction to Computer Technologies

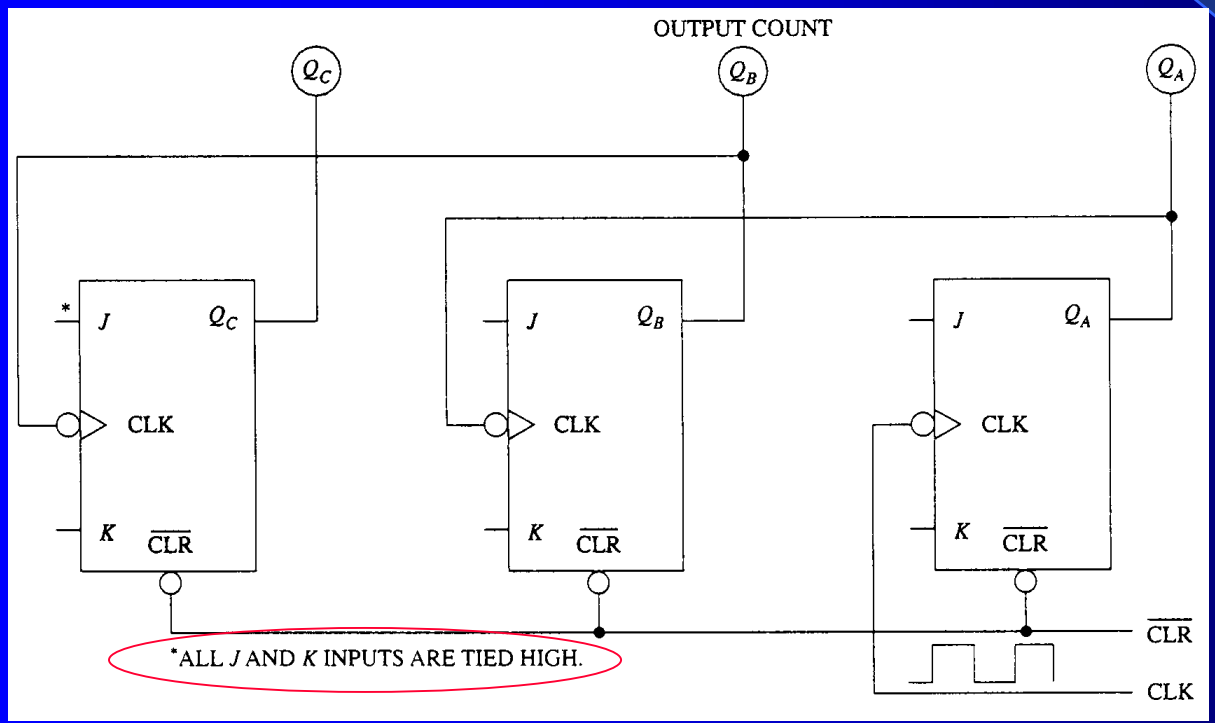
Design of Sequential Logic Circuits

Common sequential circuits

- Counters
  - A digital counter is a circuit used to generate binary numbers in a specific count sequence. That sequence is mainly governed by input clock pulses, and it is repetitive as long as these clock pulses are applied. Counters serve two main functions in digital systems – counting (for example, program counter) and frequency division.
  - ASYNCHRONOUS SYNCHRONOUS

Asynchronous Counter (Ripple Counter)

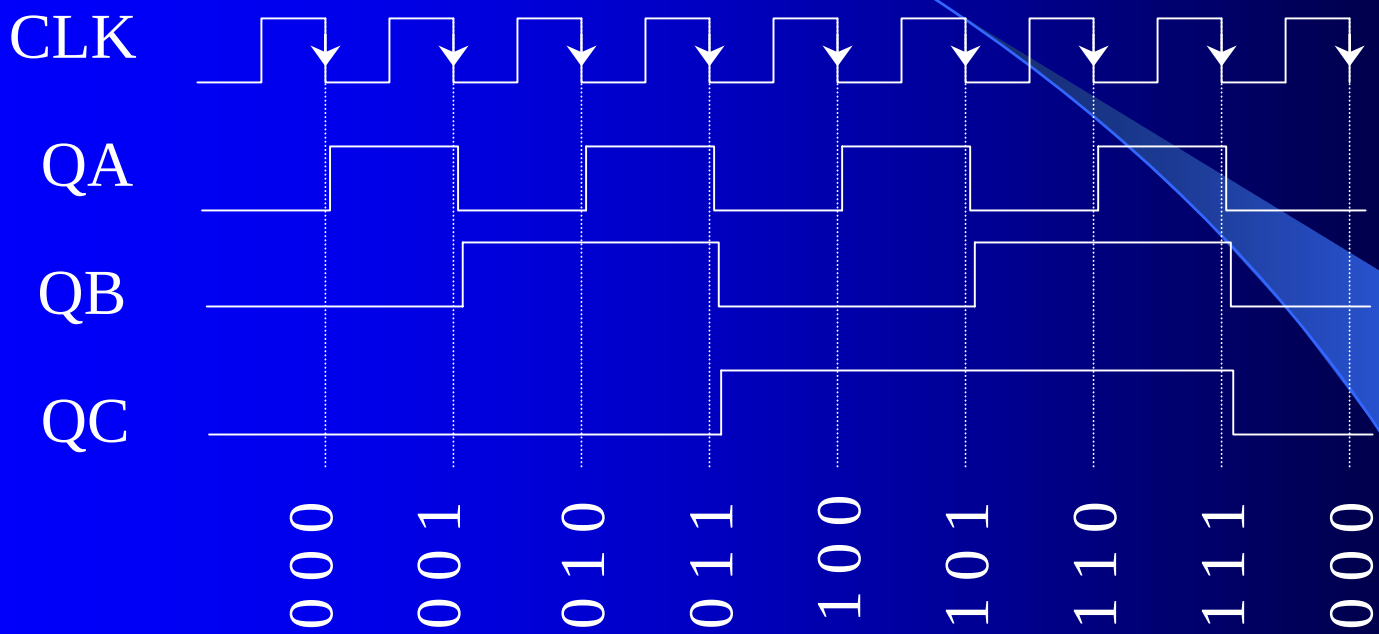
- The basic building block is a toggle flip-flop.



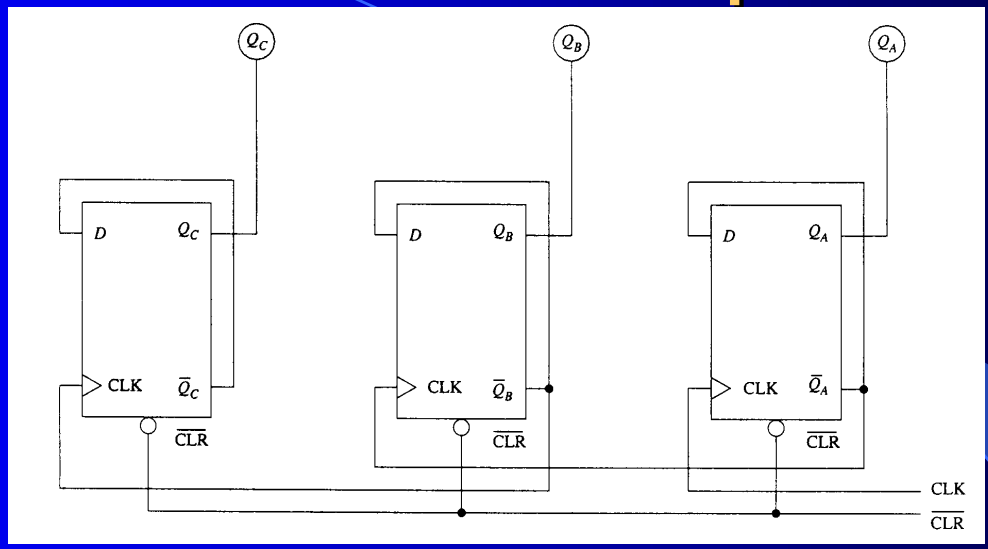
CLOCK	Q_C	Q_B	Q_A
$\overline{CLR}$	0	0	0
t_1	0	0	1
t_2	0	1	0
t_3	0	1	1
t_4	1	0	0
t_5	1	0	1
t_6	1	1	0
t_7	1	1	1

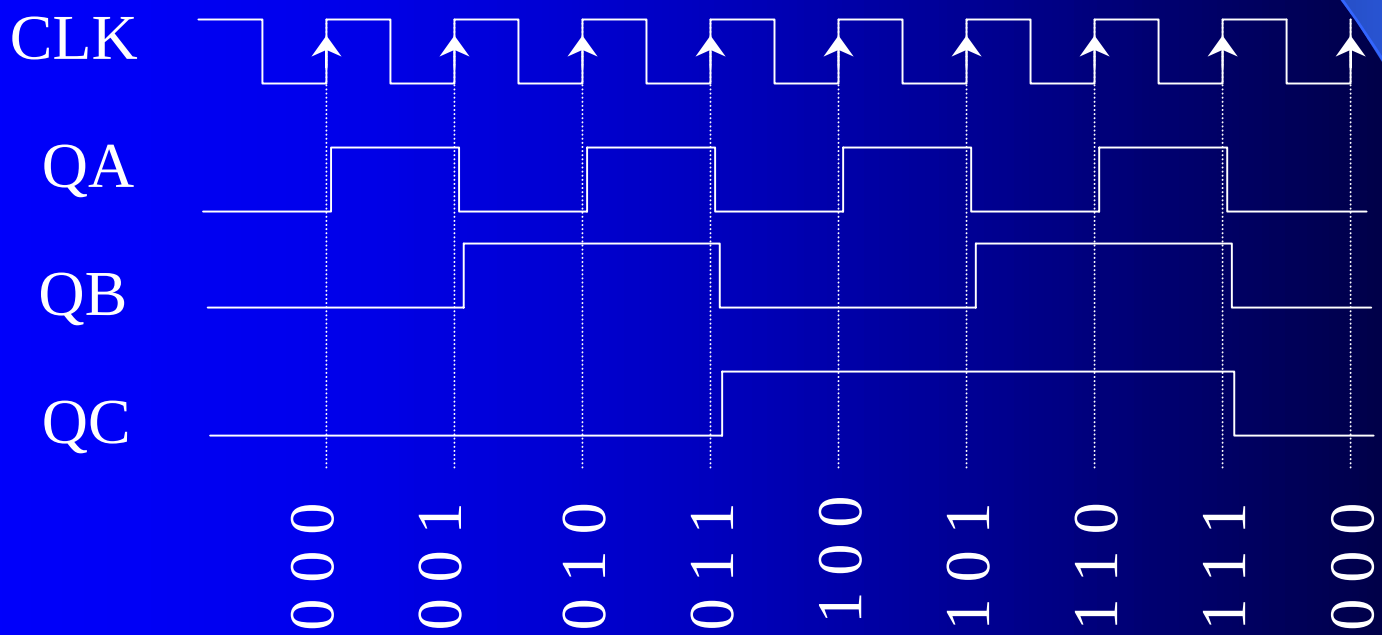
- It becomes down-counter if output is taken from $\overline{Q}$

Mod-8 Up-Counter Timing Diagram

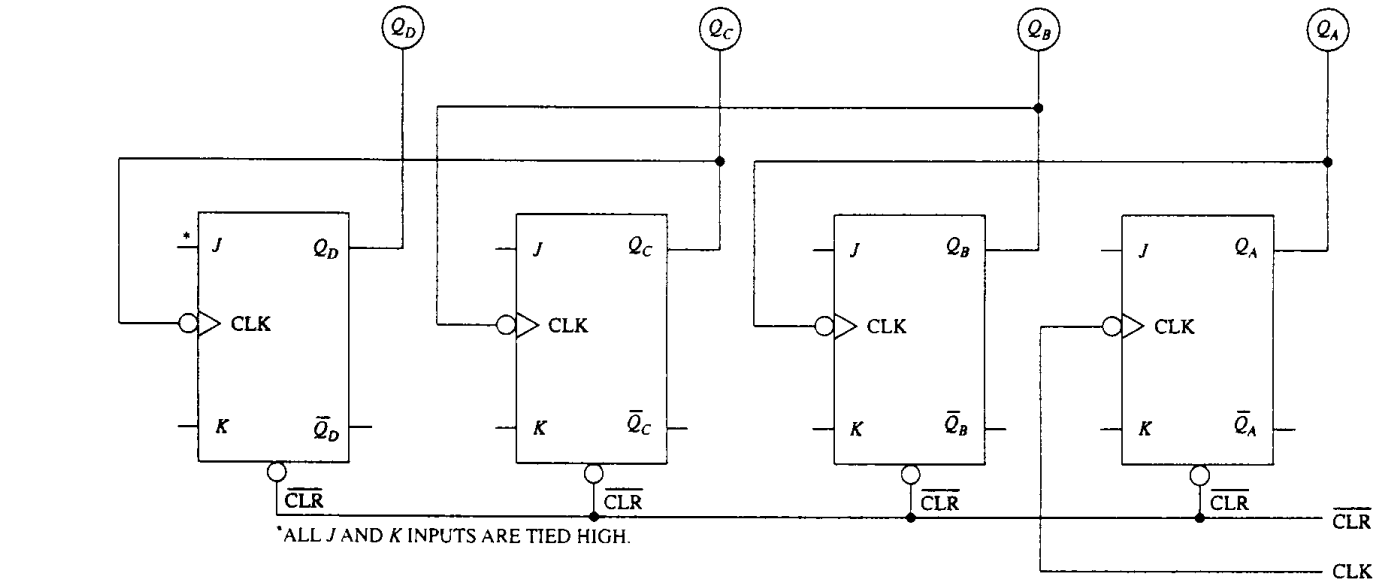


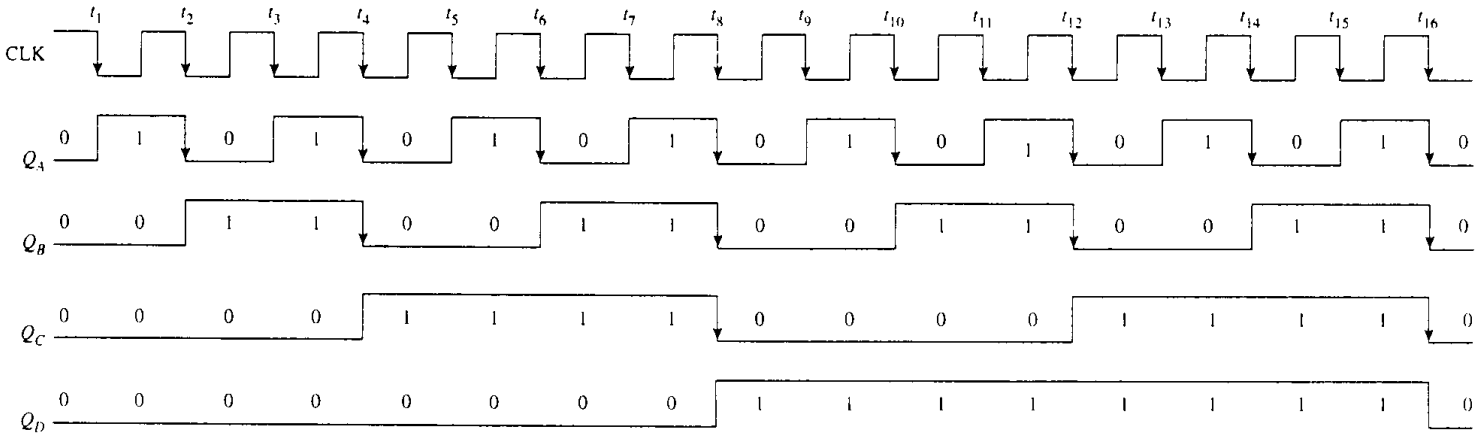
Alternative Mod-8 Up-Counter



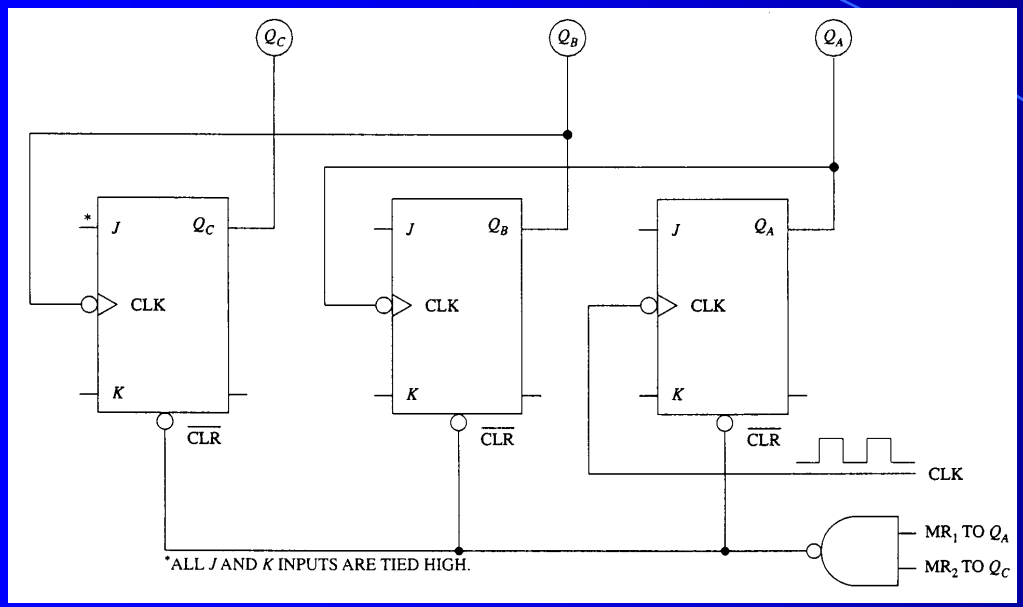


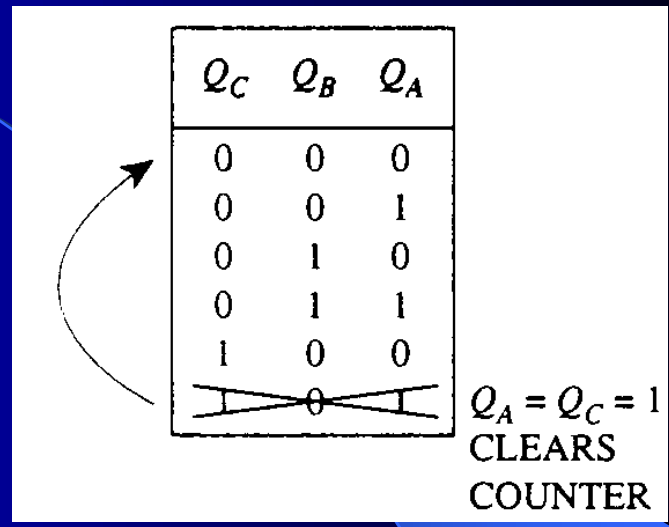
Mod-16 up counter

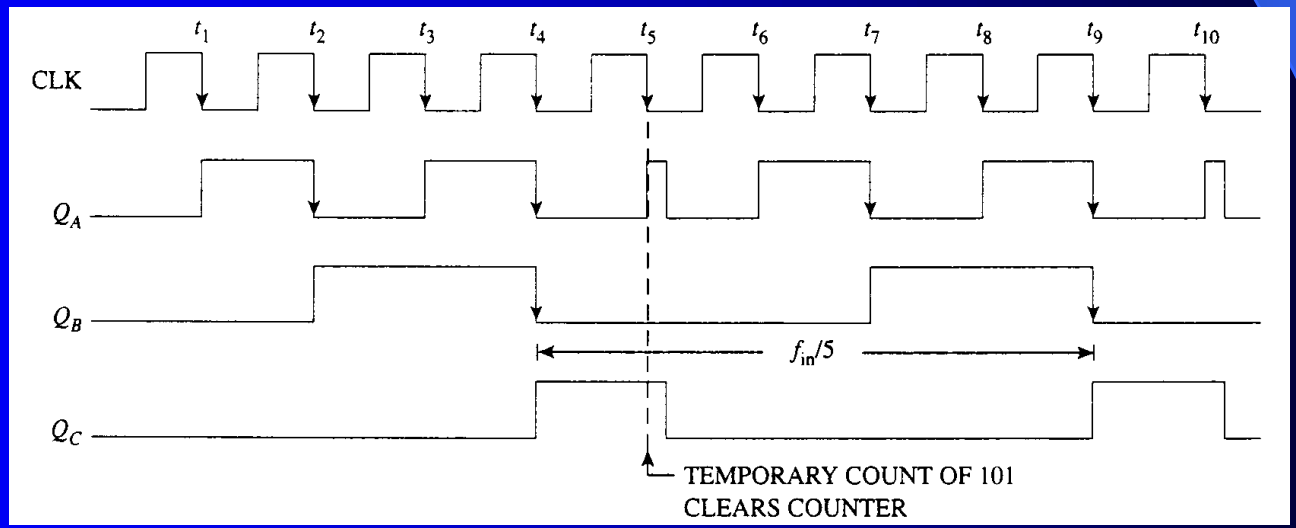




Mod-5 counter



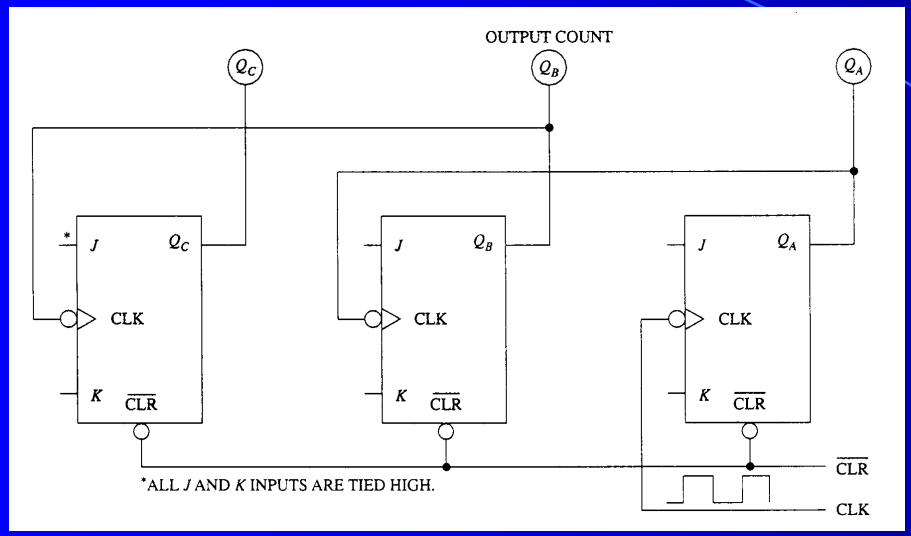




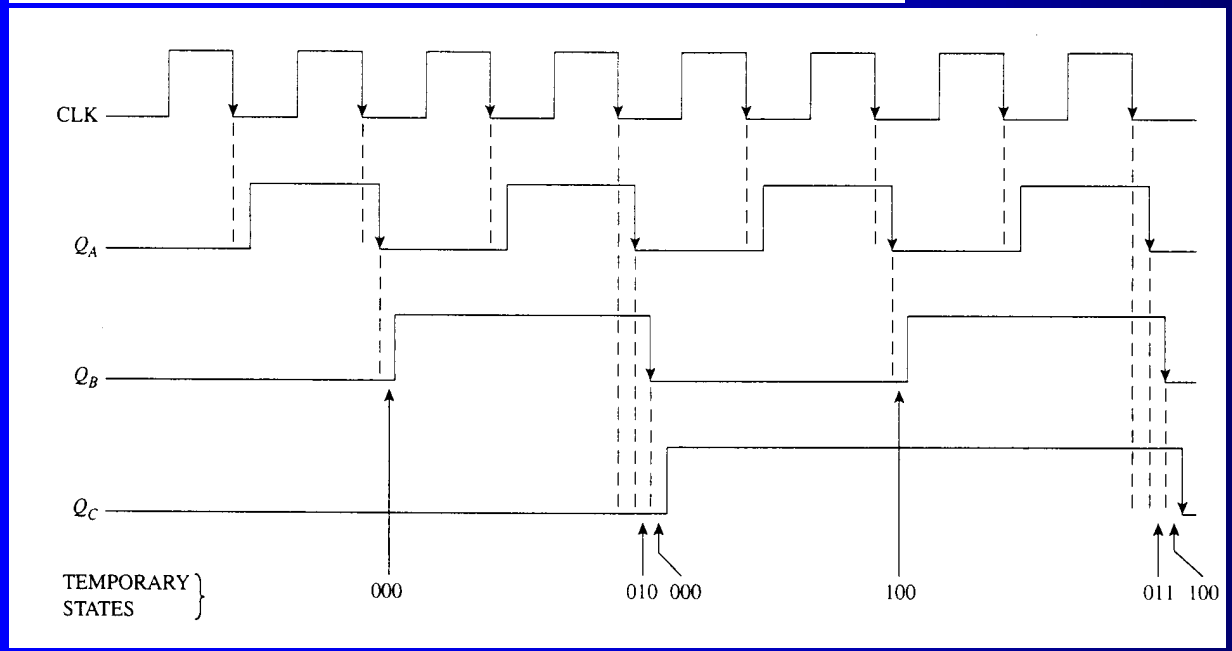
Class exercise

- Design a mod-6 up counter

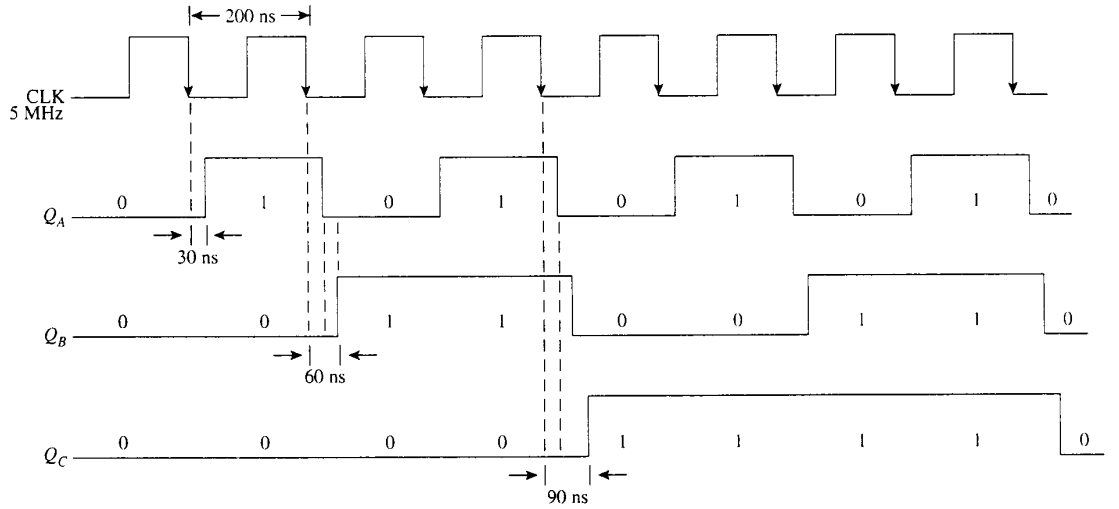
Miscounts in asynchronous counters

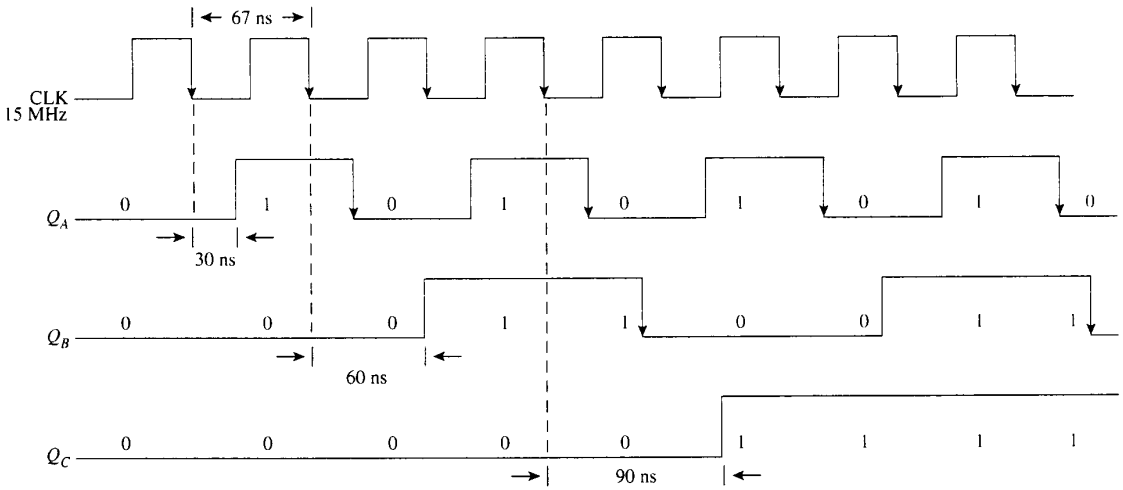


- The additive propagation delays produce short duration of miscounts.
- Can be avoided in output is read synchronously.



Maximum frequency allowed in the asynchronous counters





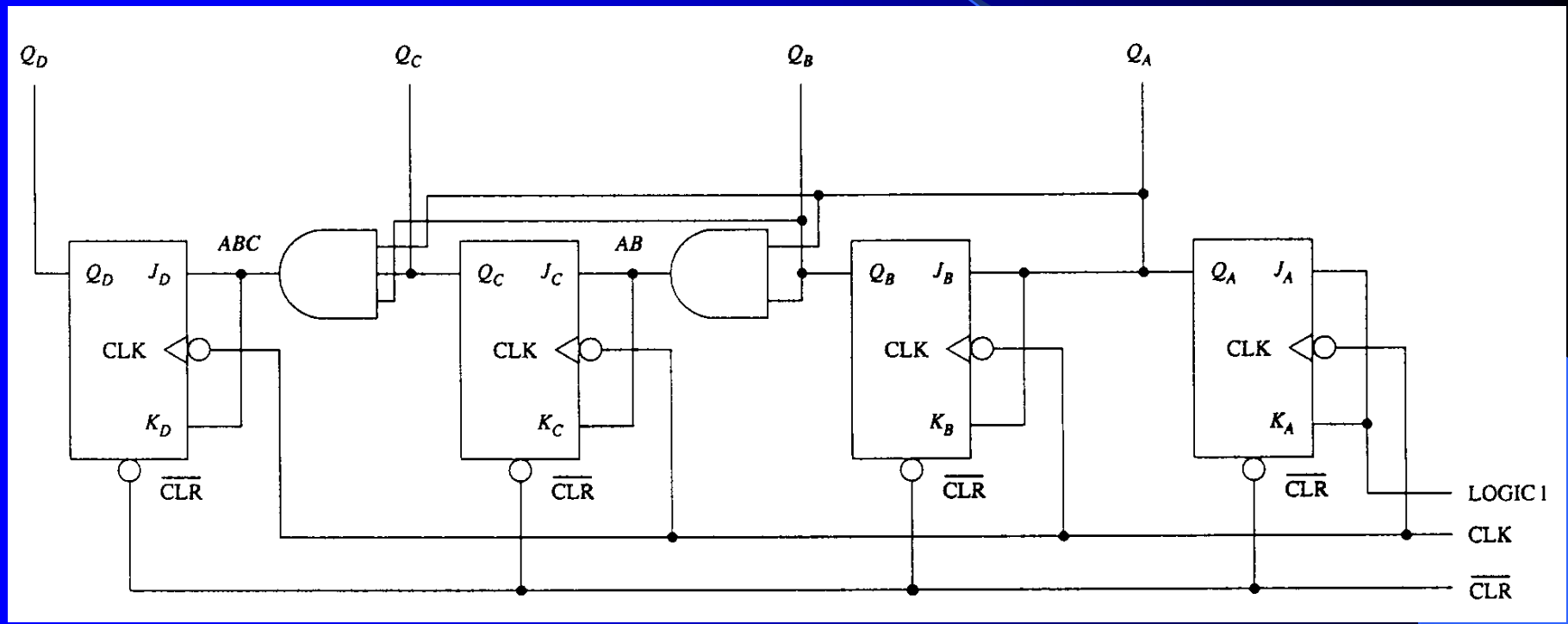
$$f_{max} = \frac{1}{n\,\tau_{ff}}$$

n – number of stages

τ_{ff} – propagation delay of flip-flop

Synchronous Counters

- All flip-flops are clocked simultaneously.



Mod-16 synchronous up-counter

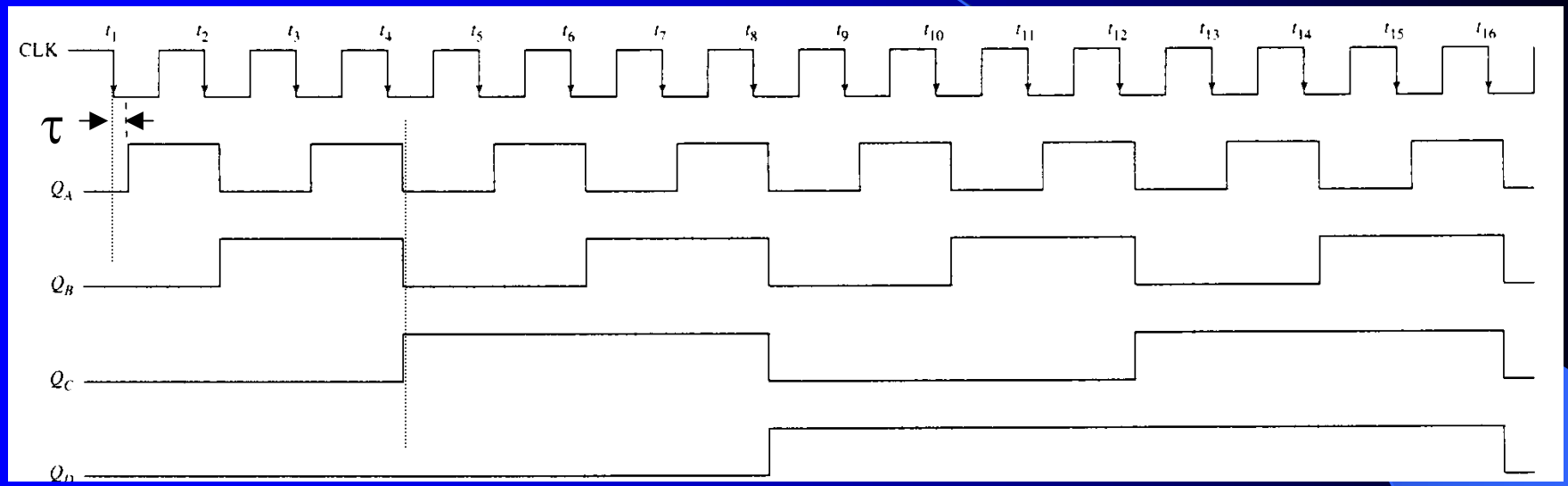
State-transition table

- QA toggles in every clock cycle;
- QB toggles when QA is 1.
- QC toggles when both QA and QB are 1.
- QD toggles when QA, QB and QC are 1.

CLOCK	Q_D	Q_C	Q_B	Q_A
CLR	0	0	0	0
t_1	0	0	0	1
t_2	0	0	1	0
t_3	0	0	1	1
t_4	0	1	0	0
t_5	0	1	0	1
t_6	0	1	1	0
t_7	0	1	1	1
t_8	1	0	0	0
t_9	1	0	0	1
t_{10}	1	0	1	0
t_{11}	1	0	1	1
t_{12}	1	1	0	0
t_{13}	1	1	0	1
t_{14}	1	1	1	0
t_{15}	1	1	1	1
t_{16}	0	0	0	0

Synchronous mod-16 up-counter

Timing diagram



No delay among QA, QB and QC

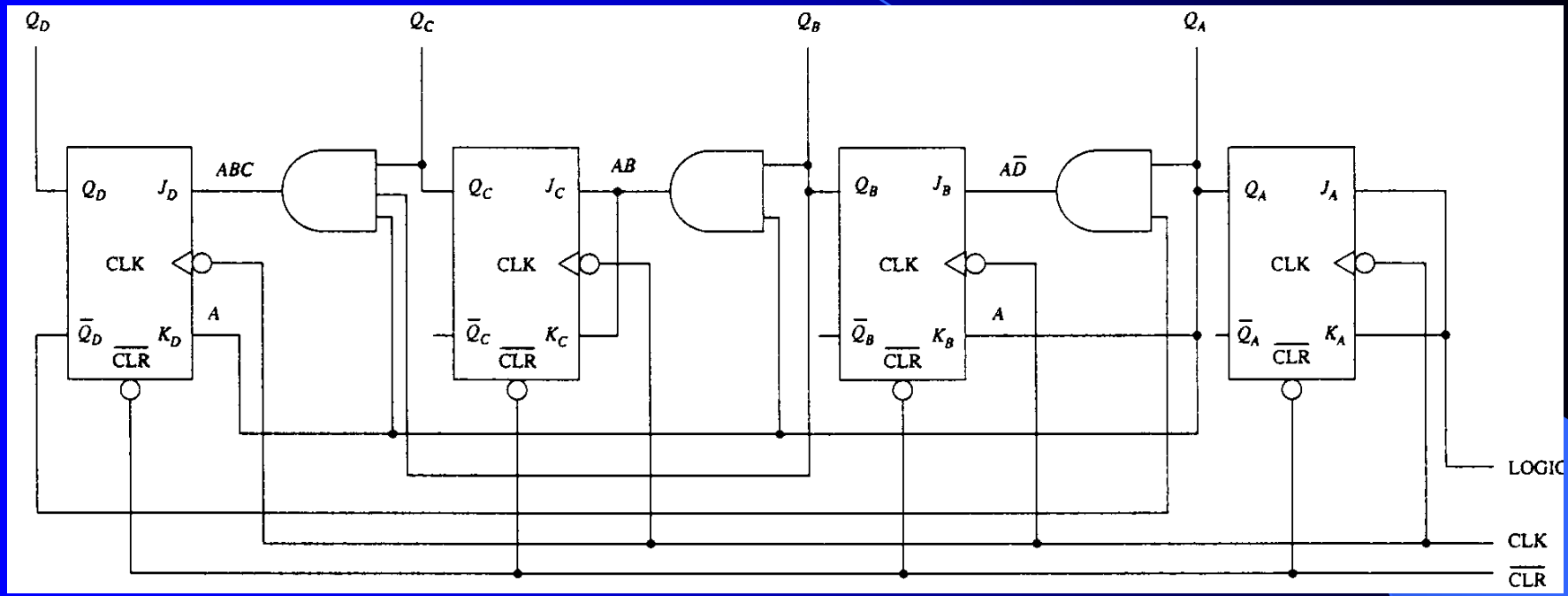
Maximum frequency: $f_{max} = \frac{1}{\tau_{ff}}$

MOD-10 Synchronous up-counter

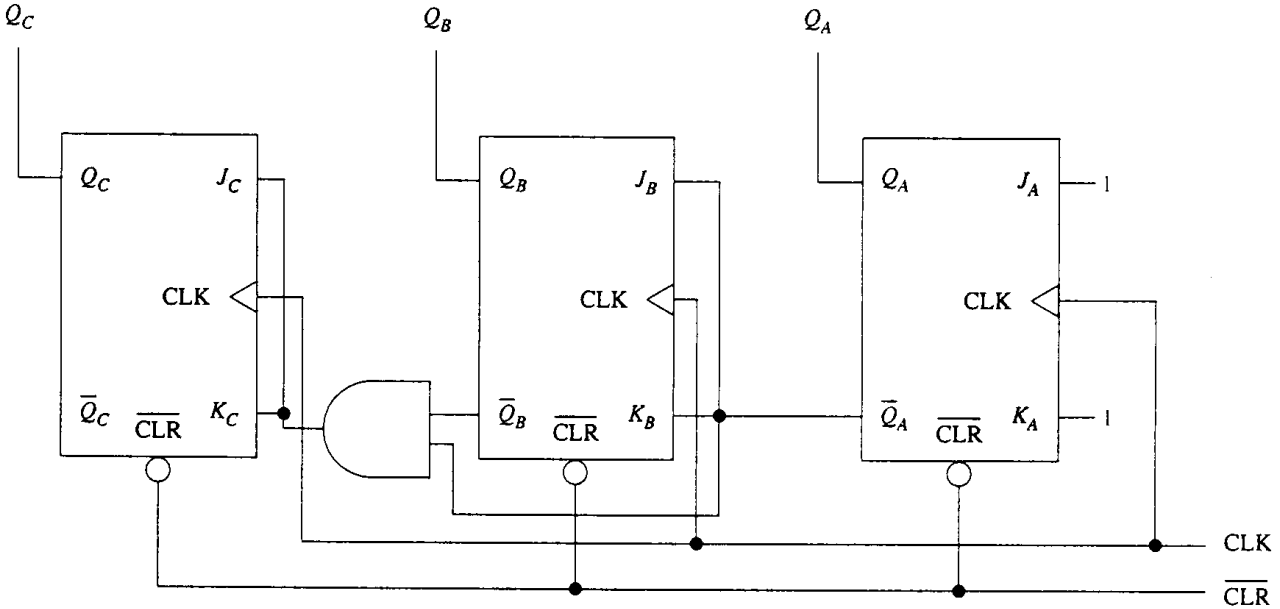
- QA – toggle every time
- QB – toggle at A high and D low
- QC – toggle at A and B high
- QD – change high at A, B and C high but change low afterwards (A high)

	Q_D	Q_C	Q_B	Q_A
	0	0	0	0
t_1	0	0	0	1
t_2	0	0	1	0
t_3	0	0	1	1
t_4	0	1	0	0
t_5	0	1	0	1
t_6	0	1	1	0
t_7	0	1	1	1
t_8	1	0	0	0
t_9	1	0	0	1
t_{10}	0	0	0	0

MOD-10 Synchronous up-counter



Mod-8 synchronous down-counter



	Q_C	Q_B	Q_A
t_0	0	0	0
t_1	1	1	1
t_2	1	1	0
t_3	1	0	1
t_4	1	0	0
t_5	0	1	1
t_6	0	1	0
t_7	0	0	1
t_8	0	0	0
t_9	1	1	1

Synchronous counter design

- Mod-6 Up-Counter Using D-flip-flops
  - Design table

TABLE

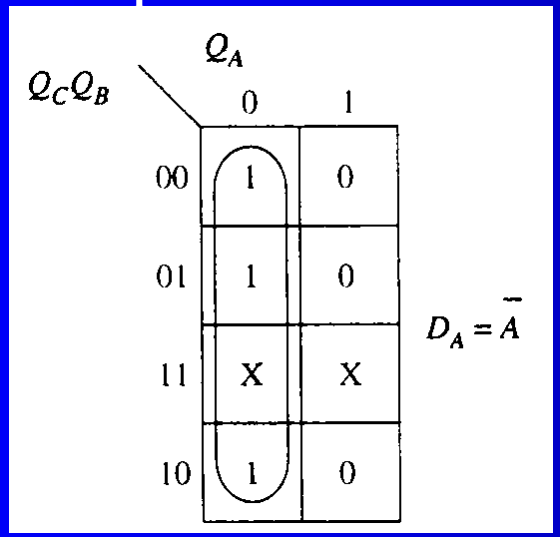
Design Table MOD-6 (D-Type Flip-Flops)

Present State	Next State	Transition Table Data		
Q^n	Q^{n+1}	Q_C	Q_B	Q_A
$Q_C Q_B Q_A$	$Q_C Q_B Q_A$	D_C	D_B	D_A
000	001	0	0	1
001	010	0	1	0
010	011	0	1	1
011	100	1	0	0
100	101	1	0	1
101	000	0	0	0

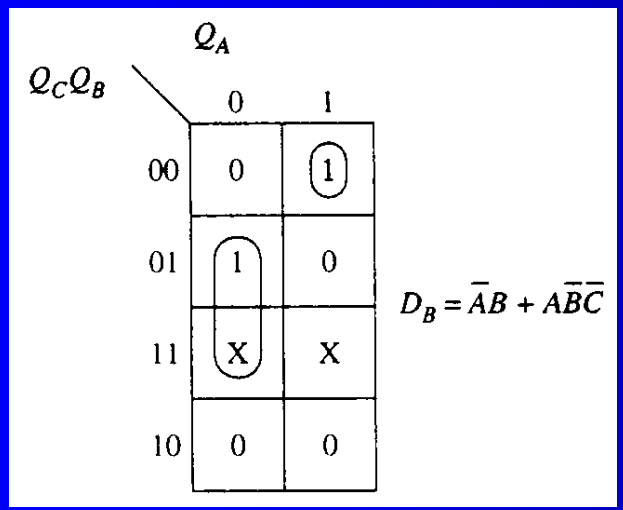
Mod-6 up-counter

– K-maps

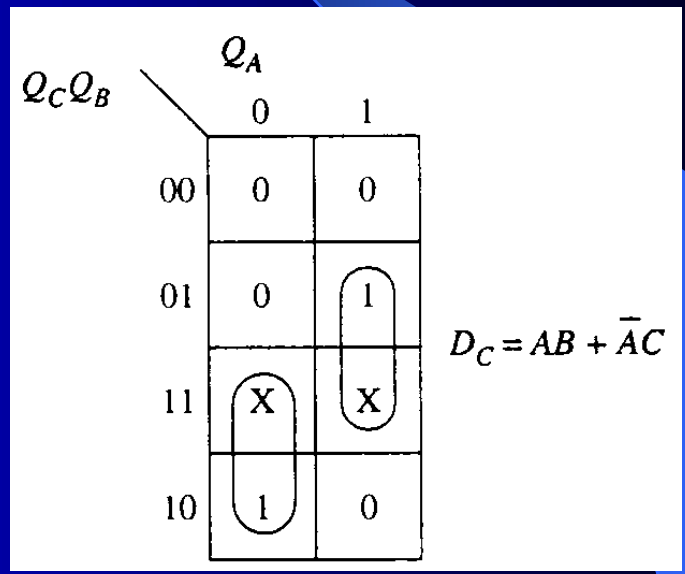
DA



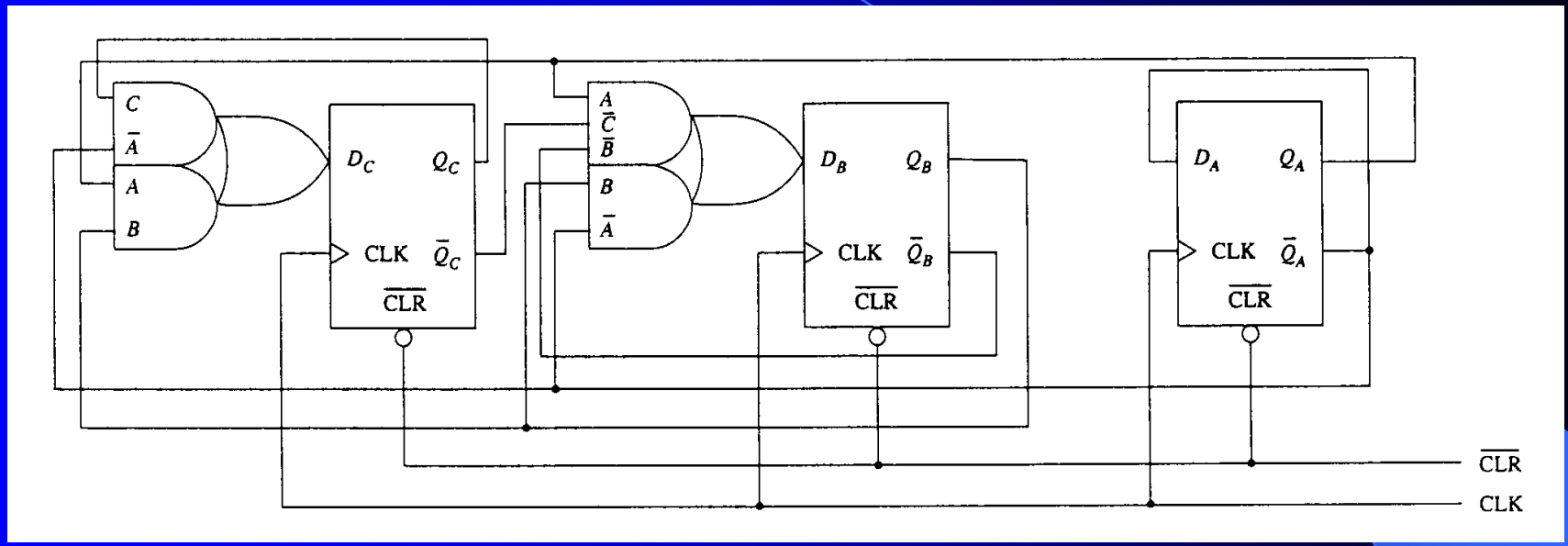
DB



DC



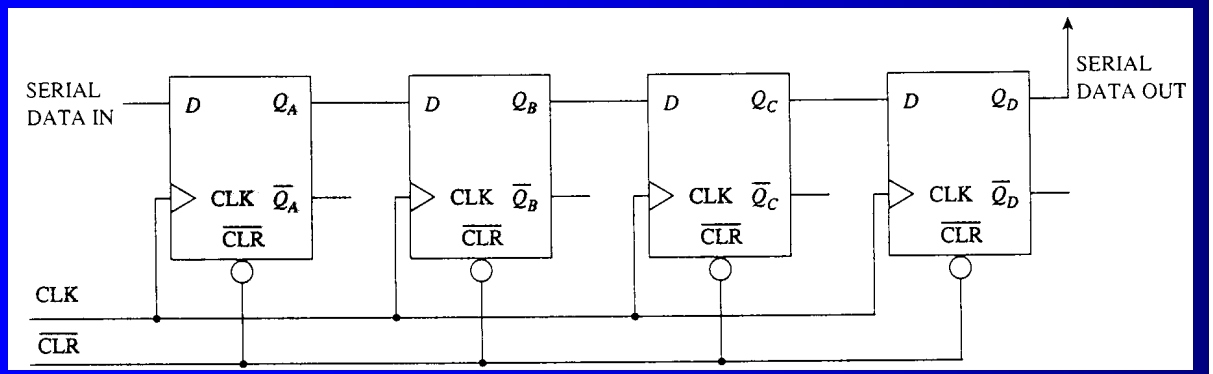
Mod-6 up-counter

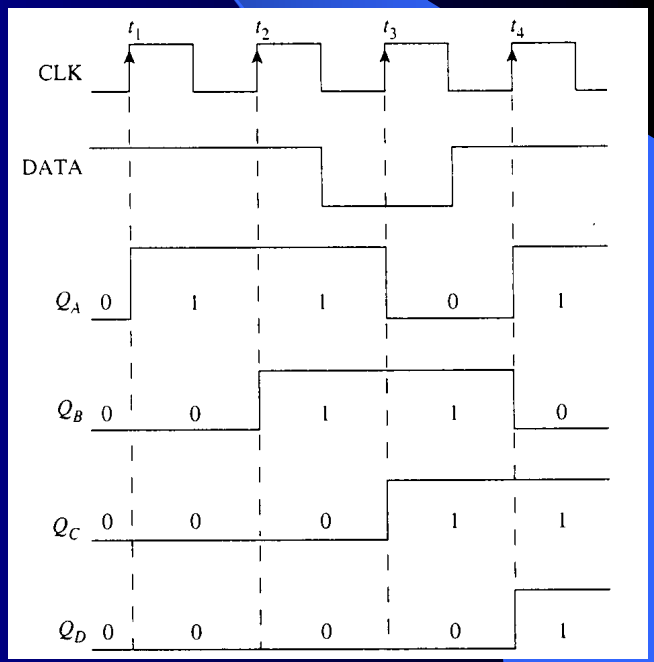


Final Design

REGISTERS

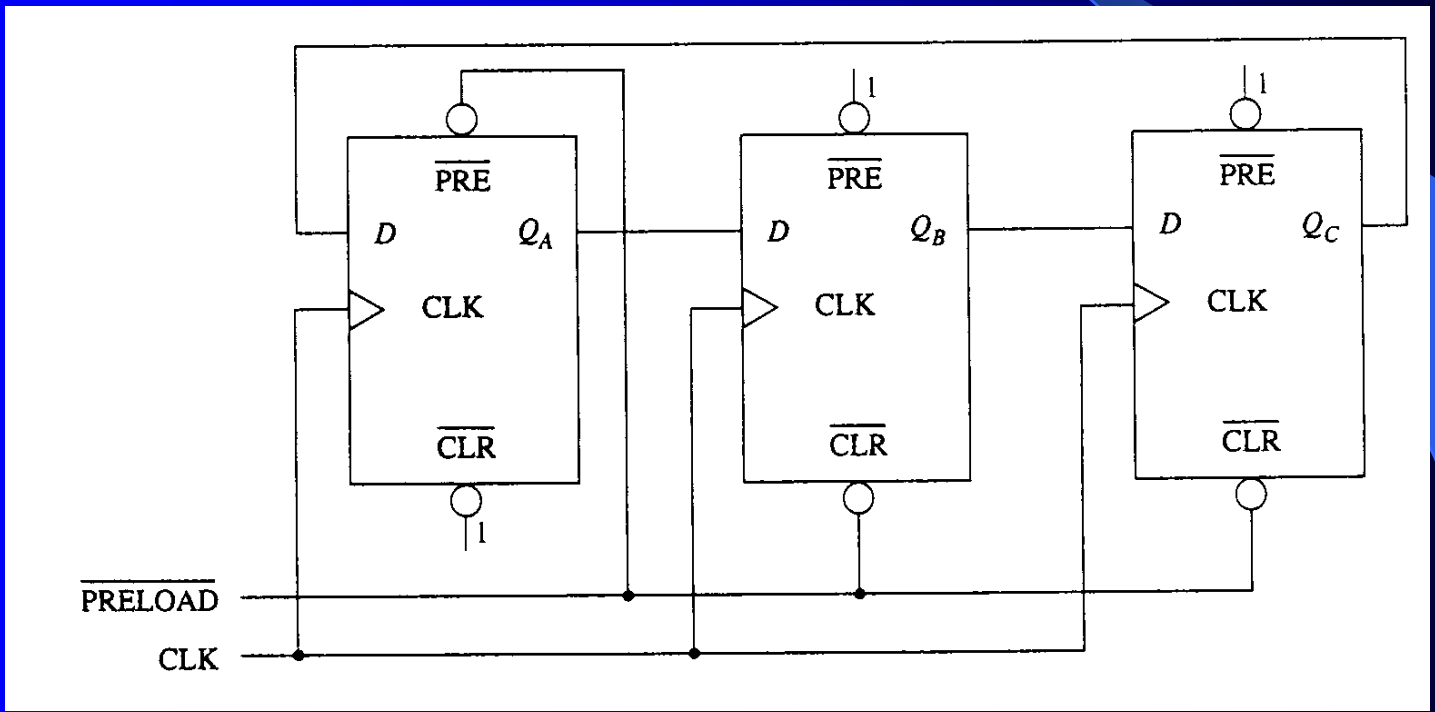
- A group of latches or flip-flops used to store, transfer, or shift data
- Serial Shift Register
  - Data is clocked into the register bit by bit





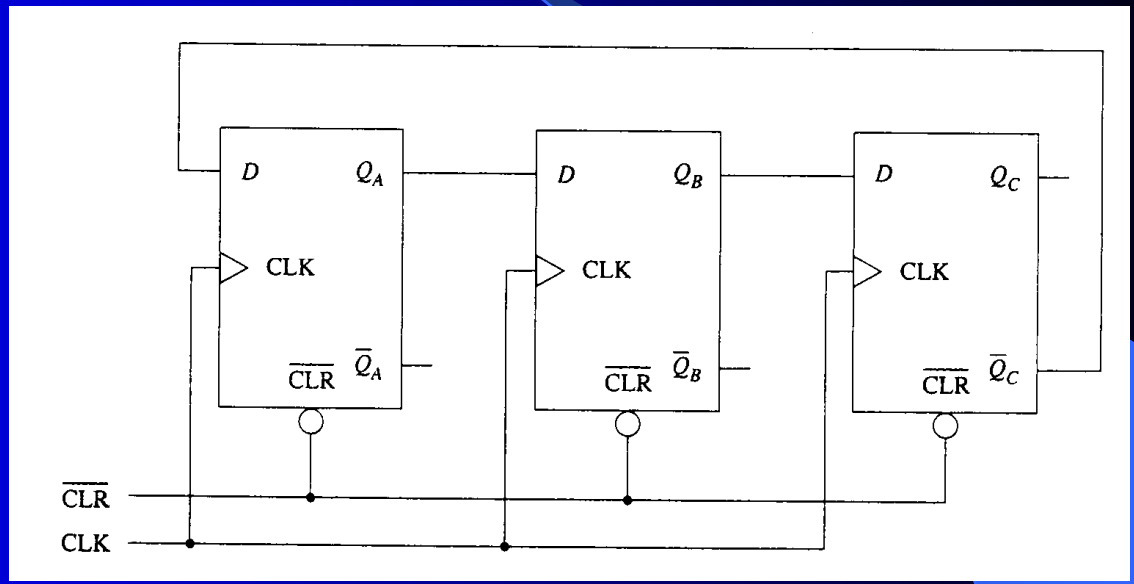
RING COUNTER

- The counter is a shift register that has its output connected back to its own input



JONHSON COUNTER

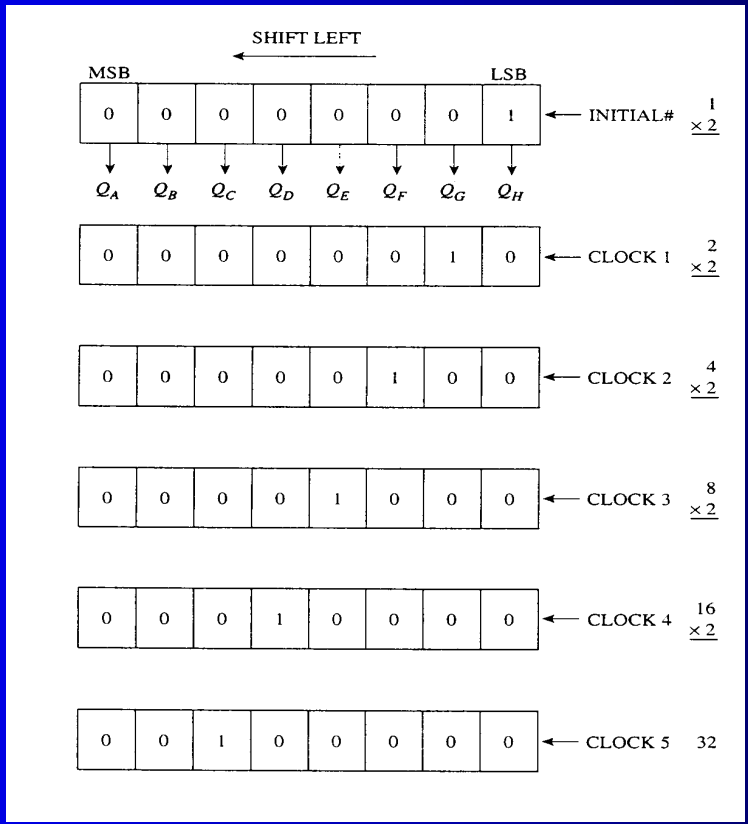
- Each bit is toggled in turn
- Mod-6
  - 000
  - 100
  - 110
  - 111
  - 011
  - 001
  - 000



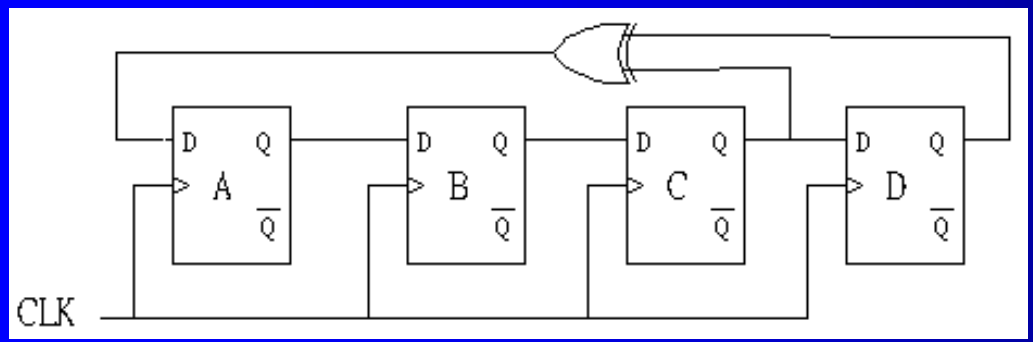
  - With its unique bit pattern, any sequence can be detected with a 2-input gate

MULTIPLY/DIVIDE REGISTER

- A left shift operation multiplies a binary number by a factor of 2
- A right shift operation divides a binary number by a factor of 2



Pseudo-random sequence generator



Q_A	Q_B	Q_C	Q_D	
0	0	0	0	INVALID CONDITION
1	0	0	0	
0	1	0	0	
0	0	1	0	
1	0	0	1	
1	1	0	0	
0	1	1	0	
1	0	1	1	
0	1	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	
0	1	1	1	
0	0	1	1	
0	0	0	1	
1	0	0	0