ITM1010
Computer and Communication Technologies

Lecture #6

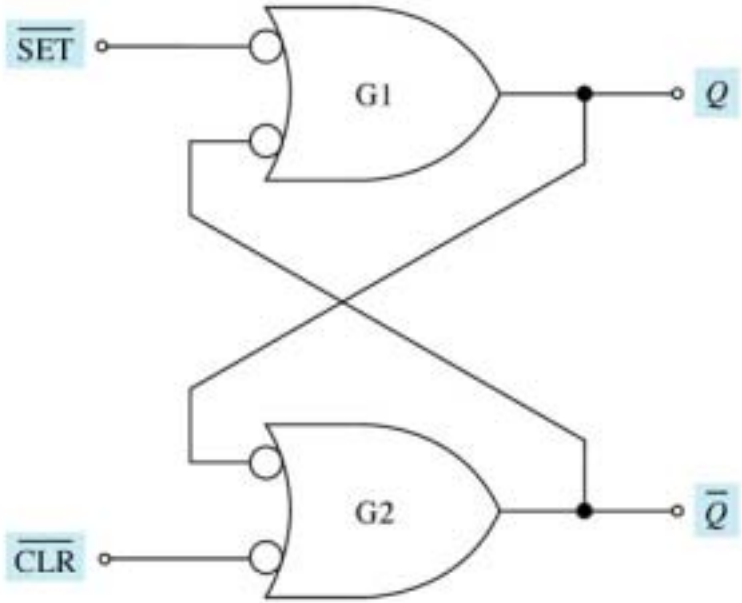
Part I: Introduction to Computer Technologies

Sequential Logic Circuits

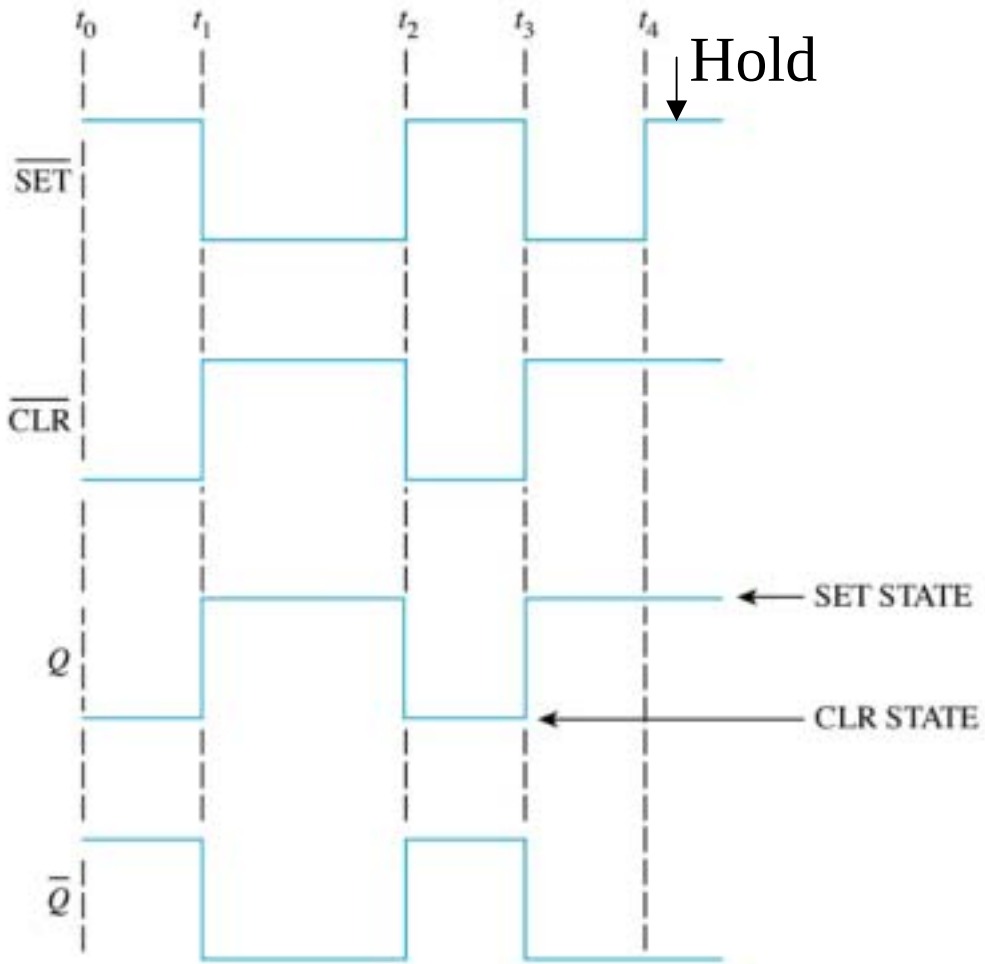
Basic components in logic circuits

- Combinational circuits
  - AND gate
  - OR gate
  - Not gate
  - etc
- Sequential circuits
  - Latches
  - D-type Flip-flops
  - JK Flip-flops
  - etc

Latch Operation



(a) LOGIC DIAGRAM



(b) WAVEFORMS

Flip-Flop Circuits

Most digital systems utilize intricate, extremely stable timing circuits to synchronize operation. For example, if an operator presses a key on the keyboard of a computer, this input to the computer is asynchronous because it is not timed with the system's clock. Therefore, a method must be used to bring this asynchronous input into the system synchronously. This synchronization circuitry often employs flip-flops.

Flip-Flop vs. Latch

- Bistable devices: SET or CLEAR
- Have a clock input.
- Edge-triggered. Flip-flops are triggered to change states only on the active transition of a clock pulse from low to high or high to low.

- Bistable devices: SET or CLEAR
- No clock input.
- Latches change output state as soon as the corresponding input changes.

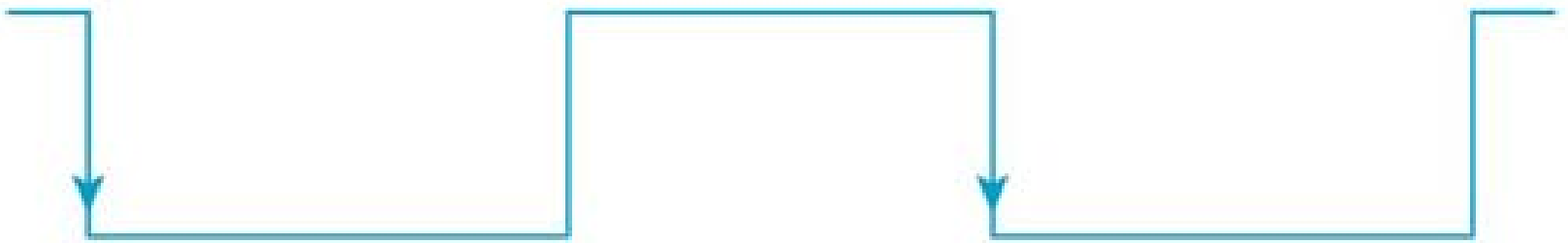
Flip-Flop Circuits

The output of a flip-flop can respond to the data inputs only on an active transition (edge) of the input clock pulse. If the flip-flop is clocked on the low-to-high clock transition, it is positive-edge triggered. This is usually referred to as the Positive-Going Transition (PGT) of the clock pulse.

(a) PGT

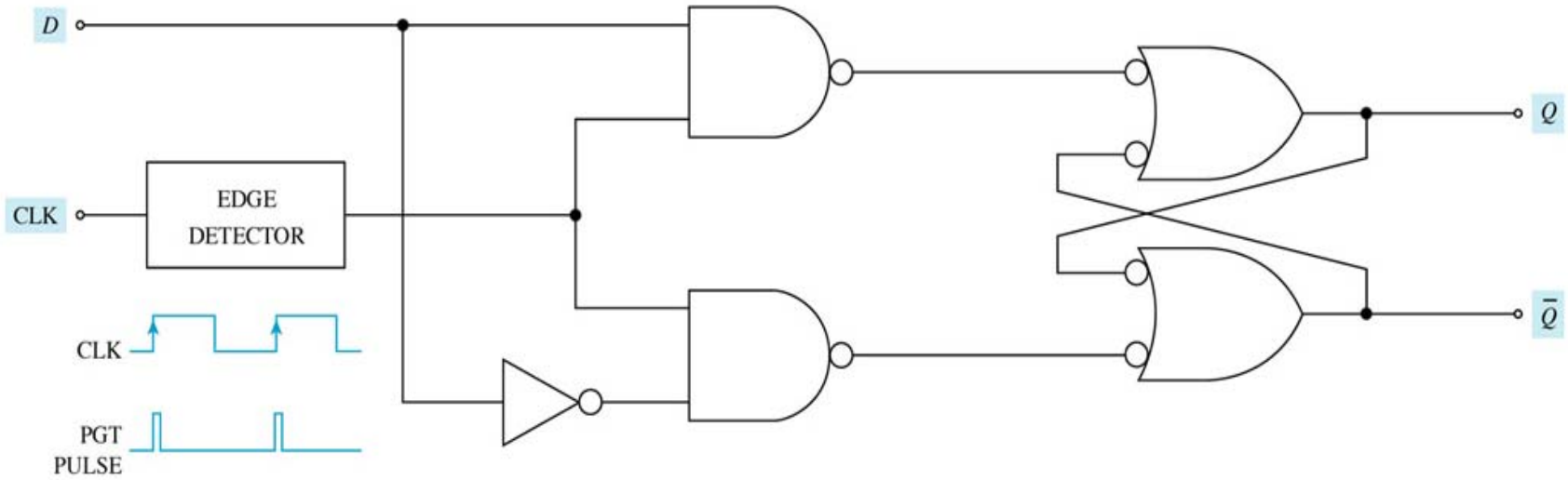
Flip-Flop Circuits

If the flip-flop is clocked on the high-to-low clock transition, the circuit is negative-edge triggered. This is normally called the Negative-Going Transition (NGT) of the clock pulse.



(b) NGT

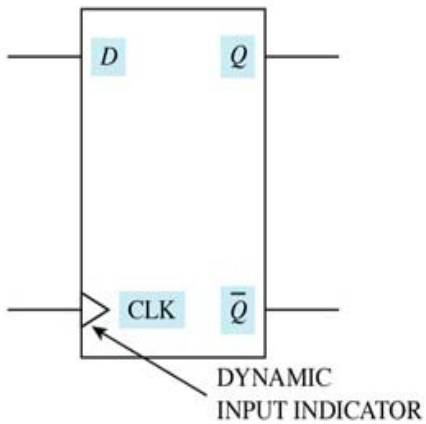
Positive-edge-triggered D-Type Flip-Flop



(a) LOGIC DIAGRAM

INPUTS		OUTPUTS	
D	CLK	Q	$\overline{Q}$
1	↑	1	0
0	↑	0	1
X	L	NC	NC

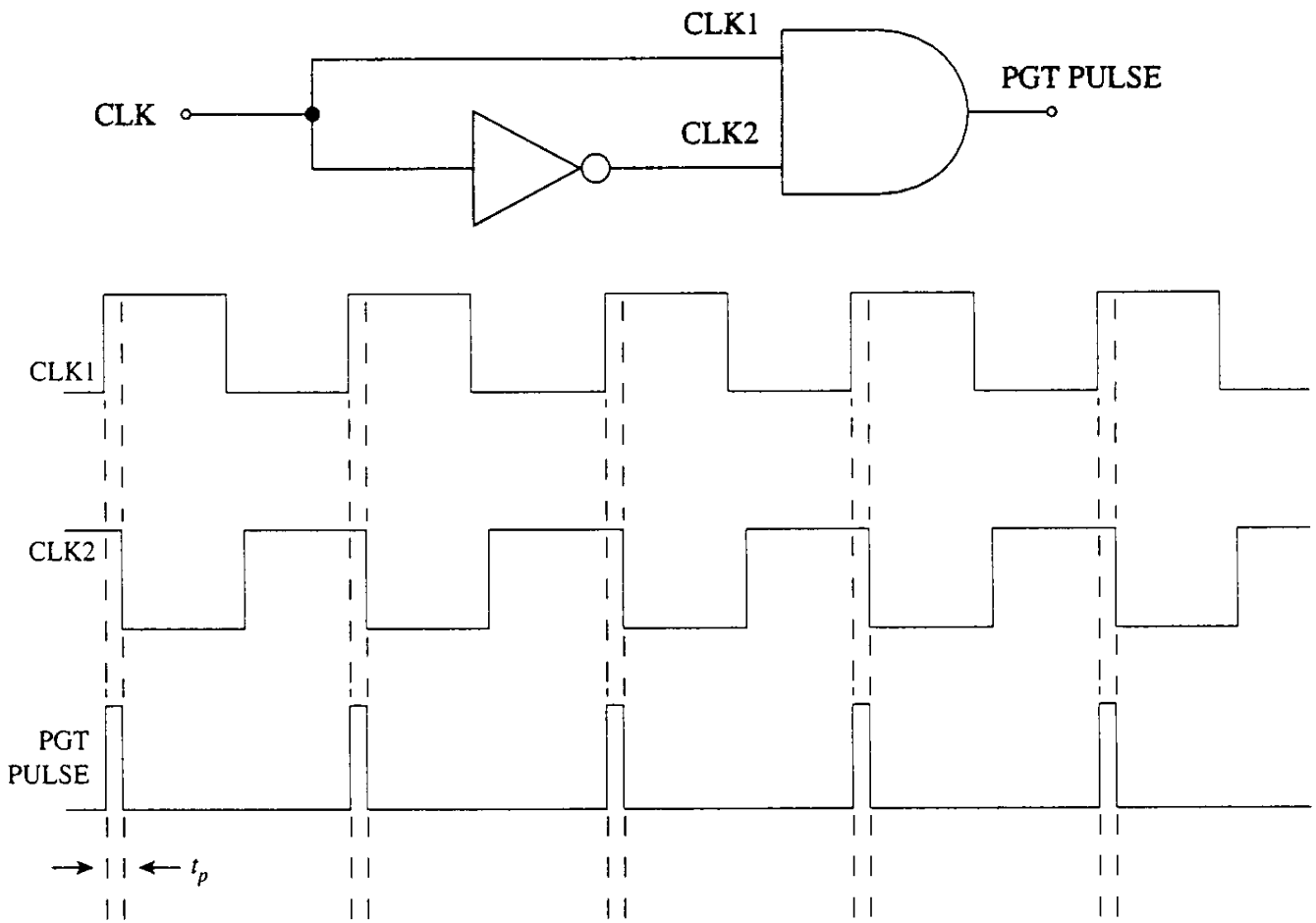
(b) STATE TABLE



(c) LOGIC SYMBOL

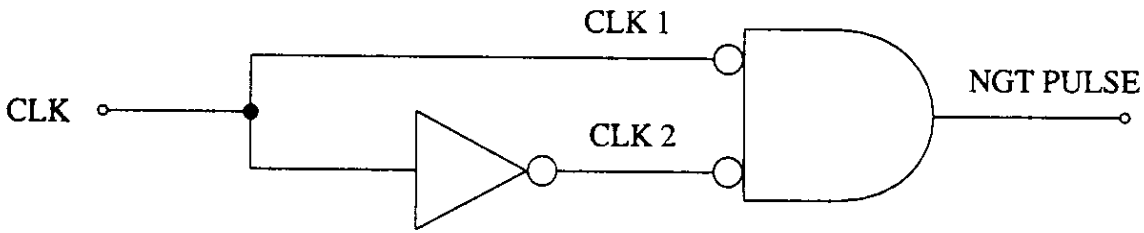
EDGE Detectors

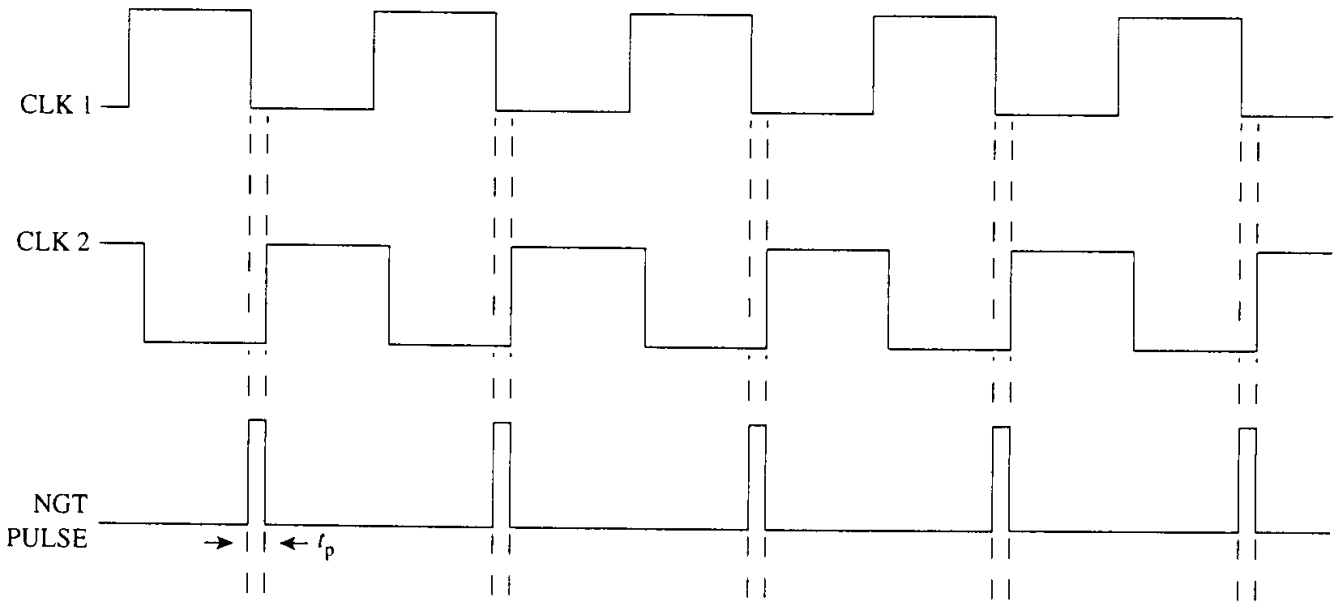
- Positive-Edge Detector



EDGE Detectors

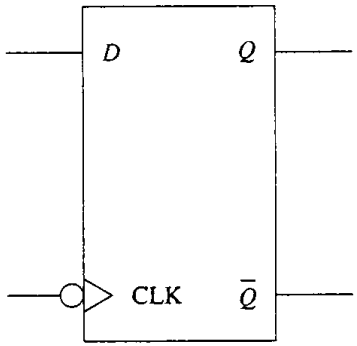
- Negative-Edge Detector



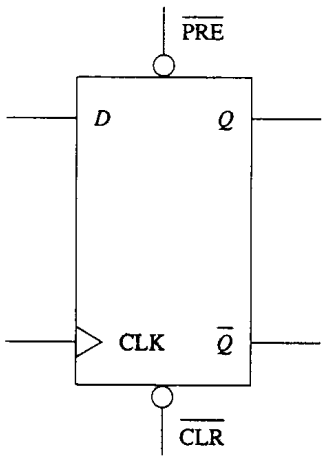


D-Type Flip-flop variants

- Negative-Edge Triggered



- With Asynchronous Controls

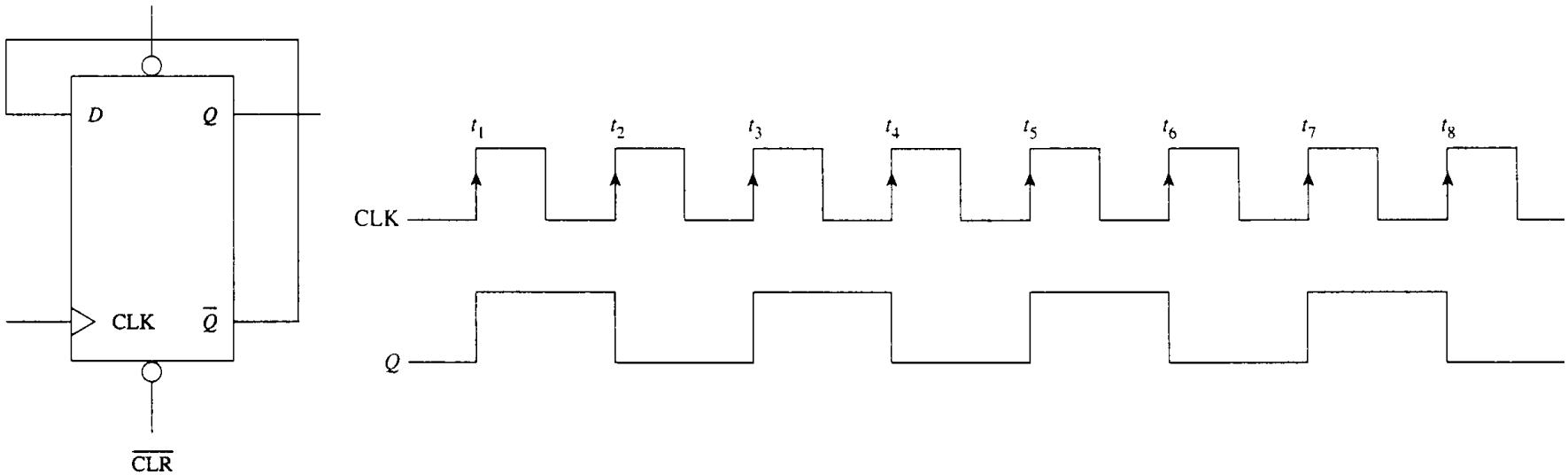


INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
0	0	X	X	1	1*
0	1	X	X	1	0
1	0	X	X	0	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	NC	NC

*INVALID

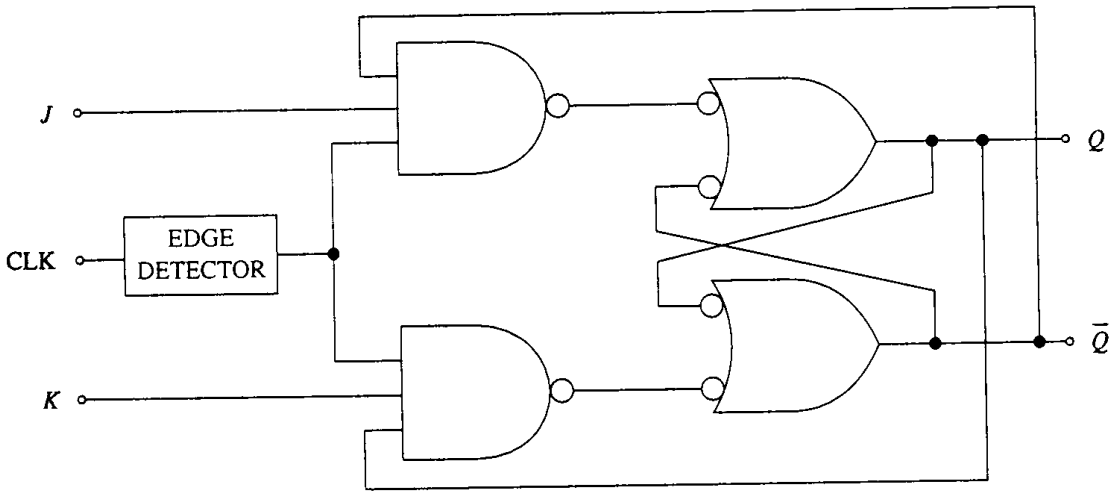
Toggle Flip-flop

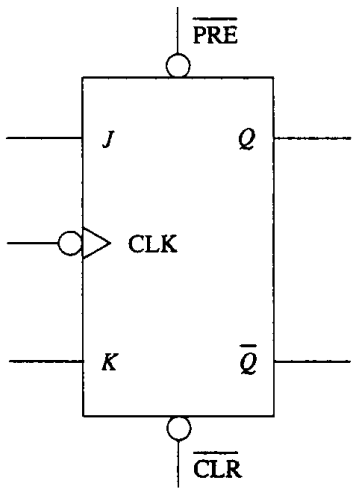
- The flip-flop changes states on every active clock transition



- From the waveform, one can observe that when a toggle flip-flop is continuously driven by a clock signal of frequency fin, the output (Q) produces a repetitive waveform of frequency fout=fin/2

J-K Flip-flop





INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1*	1*
1	1	↓	0	0	NC	NC
1	1	↓	1	0	1	0
1	1	↓	0	1	0	1
1	1	↓	1	1	TOGGLE	
1	1	1	X	X	NC	NC

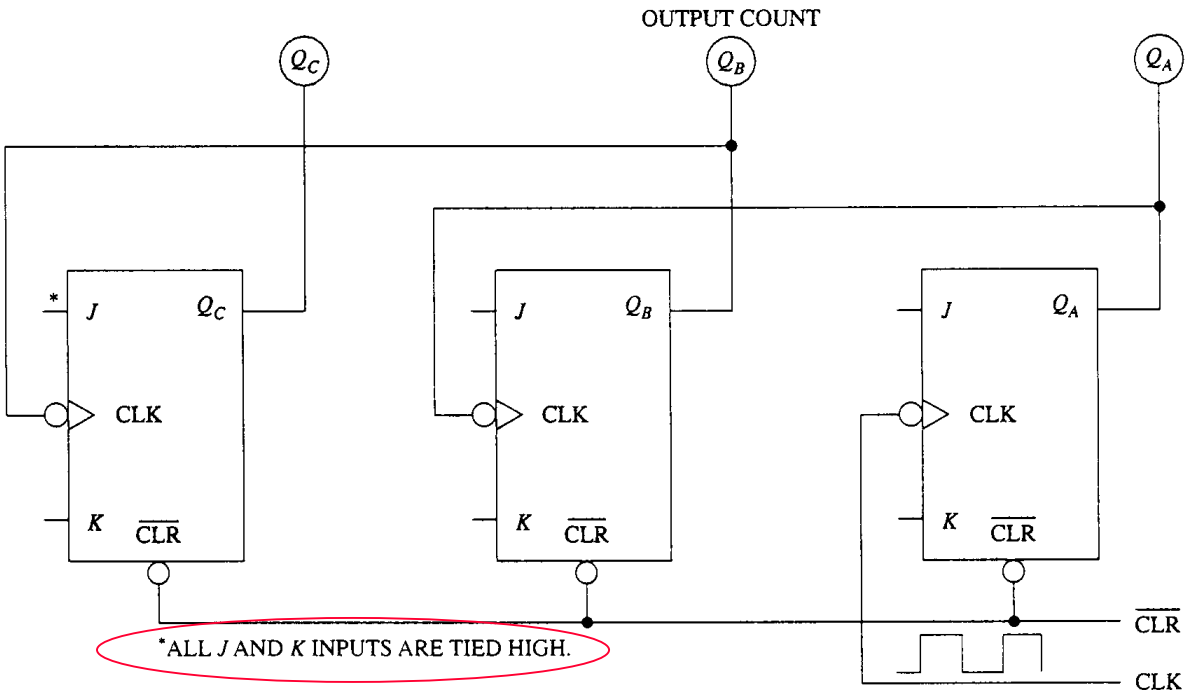
NC: no change

Common sequential circuits

- Counters
  - A digital counter is a circuit used to generate binary numbers in a specific count sequence. That sequence is mainly governed by input clock pulses, and it is repetitive as long as these clock pulses are applied. Counters serve two main functions in digital systems – counting (for example, program counter) and frequency division.
  - ASYNCHRONOUS SYNCHRONOUS

Asynchronous Counter (Ripple Counter)

- The basic building block is a toggle flip-flop.



CLOCK	Q_C	Q_B	Q_A
$\overline{CLR}$	0	0	0
t_1	0	0	1
t_2	0	1	0
t_3	0	1	1
t_4	1	0	0
t_5	1	0	1
t_6	1	1	0
t_7	1	1	1

Delay problem

- Since each flip-flop receives its clock pulse from another flip-flop, there will be delay through these flip-flops. This delay is the longest for the MSB flip-flop.
- In the 3-stage counter, if each flip-flop has a propagation delay of 10 *ns* (1*ns*=10^{-9} s), then the maximum clock frequency f_{max} that can be used is:

$$f_{max} = 1/(3x10ns)=33.3MHz$$

Alternative Mod-8 Up-Counter