ITM 1010
Computer and Communication Technologies

Lecture #21
Review: Computer Technologies

Review of Computer Technologies

- Number systems and codes
- Boolean Algebra
- Combinational Logic Circuits
  - Logic Gates
  - POS and SOP expressions
  - K-map
  - Common combinational circuits
- Sequential Logic Circuits
  - Latches and Flip-flops
  - Asynchronous counters
  - Synchronous counters
- Computer Organization

Number systems and codes

- Convert a decimal number to binary and vice versa
- Represent a negative number in 1's complement and 2's complement formats, and perform subtraction by using 2's complement
- Convert a decimal number to Hexadecimal and BCD, and vice versa
- The objective and property of Gray code; Counting sequence in gray code.
- ASCII code

Boolean Algebra

- Basic Operators: Or, And, Not
- Venn Diagram
- DeMorgan's Theorem
- Basic Logic Gates: OR, AND, NOT, XOR, ...
- Truth table
- Extract logic expression from a truth table in the following formats:
  - Sum-of-Product (SOP)
  - Product-of-Sum (POS)
- Minimize logic expressions by using
  - Boolean algebra
  - K-map

Common Combinational Logic Circuits

- BCD Encoder
- Multiplexer
- DeMultiplexer
- Half Adder
- Full Adder
- Multi-bit Adder and Subtractor

Sequential Logic Circuits: Latches and Flip-flops

- Latches:
  - NAND-gate Latch and NOR-gate Latch
  - Four states of latches: SET, CLEAR, RETAIN, INVALID
  - State tables of active high and active low latches

- Flip-flops:
  - Change output state only at the transition edge of the clock
  - D-type flip-flop
  - J-K flip-flop, four states: SET, CLEAR, RETAIN, TOGGLE
  - State tables of flip-flops

Sequential Logic Circuits: Asynchronous Counters

- Built on toggle flip-flops
- Design a Mod-n up/down counter
- Problems:
  - Delay
  - Miscount
- Maximum clock frequency allowed:

$$f_{max} = \frac{1}{n \tau_{ff}}$$

Sequential Logic Circuits: Synchronous Counters

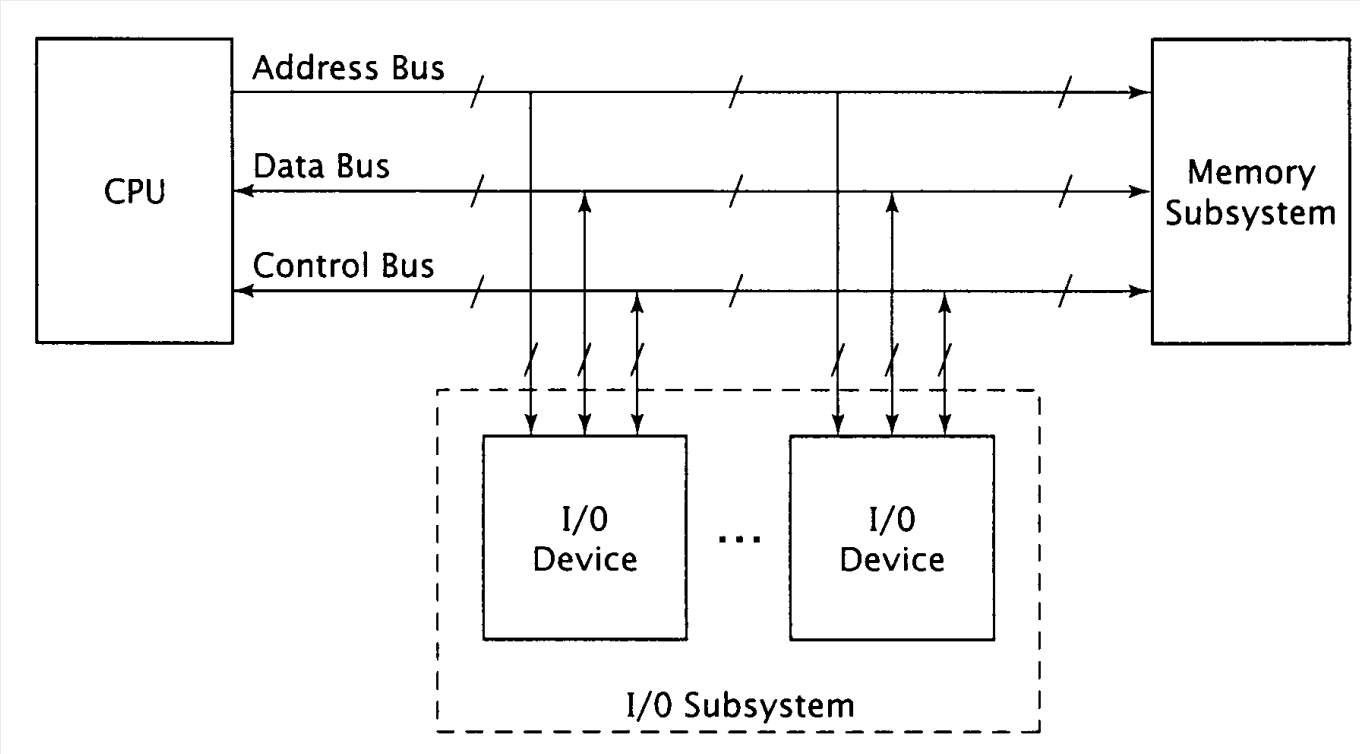
- All flip-flops are connected to the same clock
- Main advantage over asynchronous counter: high maximum clock frequency:

$$f_{max} = \frac{1}{\tau_{ff}}$$

- Design procedures for a Mod-n up/down counter using D-type flip-flop
  - Write down the state transition table
  - Construct a K-map for the input of each flip-flop
  - Minimize the logic expressions of the flip-flop inputs
  - Construct the circuits
- Other circuits: register, ring counter, Johnson counter, Pseudo-random number generator

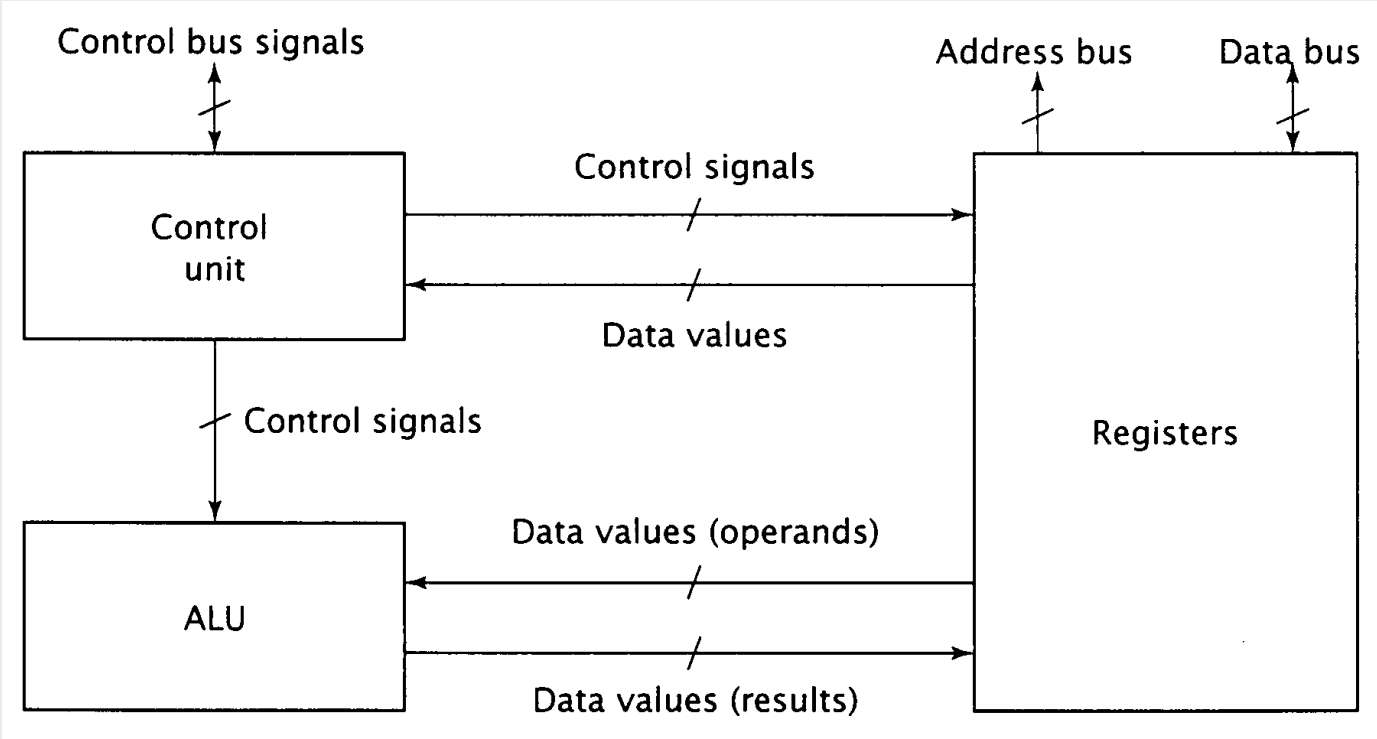
Computer Organization

- Draw the generic computer organization:



Computer Organization: CPU internal organization

- Draw the block diagram of the CPU internal organization



Computer Organization: Memory and I/O subsystem organizations

- Types of memories: RAM, ROM, EEPROM
- Control circuits of memories
- Multi-byte data organization
  - Big-Endian and Little-Endian processors
- Properties of cache memory and Virtual memory

- Interface circuits for input, output and I/O devices