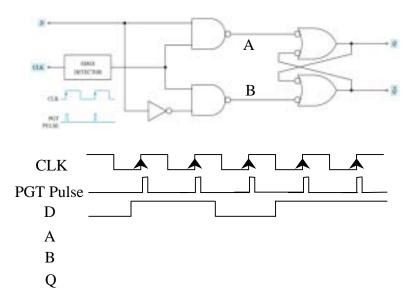
ITM1010 Assignment #2

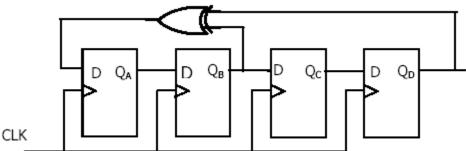
Due time: 5:00pm on Thursday, 16 October 2003 to the tutor or me.

Q1. The waveforms of CLK and D inputs of the logic circuit are given below.

Complete the waveforms at internal node A, B and the waveform of output Q.



- Q2. For the logic circuit shown below,
 - (a) Assuming $Q_A = Q_B = Q_C = Q_D = 1$, list the sequence of outputs $Q_A Q_B Q_C Q_D$
 - (b) Which states are missing in the sequence listed in (a)?
 - (c) List the sequence if the circuit were initially in one of these missing states.



- Q3. (a) Design a MOD-12 asynchronous up-counter.
 - (b) Design a MOD-8 asynchronous down-counter.
 - (c) Design a MOD-12 synchronous up-counter using D-type flip-flop.
 - (d) Design a synchronous counter that outputs the following sequence: 000, 001, 010, 011, 111, 110, 100 (repeat 000).
 - (e) Assume all the flip-flops that you have used have a propagation delay of 15ns. What are the maximum clock frequencies of your design in part (a)-(d) respectively?