ITM1010 Assignment #1

Due time: 5:00pm on Thursday, 2 October 2003 to the tutor or me.

Q-1. Convert the following decimal numbers to their binary equivalents:

a. $162_{(10)}$ **b**. $2048_{(10)}$ **c**. $32.125_{(10)}$

Q-2. Convert the following binary numbers to their decimal equivalents:

a. $101010_{(2)}$ **b**. $11011011_{(2)}$ **c**. $11101.11_{(2)}$

Q-3. Convert the following decimal numbers to their hexadecimal equivalents:

a. $426_{(10)}$ **b**. $5000_{(10)}$ **c**. $65535_{(10)}$

Q-4. Write the following decimal numbers to 3-digit hexadecimal numbers using the 2s complement representation of negative numbers (without sign bit).

a. $-1800_{(10)}$ **b**. $-3022_{(10)}$

Q-5. Subtract the following binary numbers using 2s complement. Show your work in steps.
a. $1010_{(2)}$-$1100_{(2)}$ **b**. $1010_{(2)}$-$0100_{(2)}$

Q-6. State the purposes of Gray code, BCD code and ASCII code.

Q-7. Draw the standard logic symbol for a 2-input (a) AND gate, (b) OR gate, (c) NAND gate, (d) NOR gate, and (e) XOR gate.

Q-8. Fill in the following truth tables:

Inputs		**Outputs**				
A	*B*	**AND**	**OR**	**NAND**	**NOR**	**XOR**
0	0					
0	1					
1	0					
1	1					

Q-9. Complete the following:

a. $A(B+C) =$ **b**. $A + AB =$ **c**. $A + \bar{A}B =$ **d**. $\overline{A + B} =$

Q-10. Simplify the following expressions using Boolean algebra:

a. $\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C}$

b. $\overline{A}B\overline{C} + A\overline{B}C + \overline{A}BC + A\overline{B}\overline{C}$

c. $\overline{ABC} + \overline{\overline{A} + C}$

d. $\overline{X\,\overline{\overline{Y}\,\overline{Z}}}$

Q-11. Plot the high output from the truth table on a K-map and simplify the resultant expression.

a.

A	***B***	***C***	***F***
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

X: Don't care

b.

A	***B***	***C***	***D***	***F***
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	x
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Q-12. Design a 3-input circuit that will output low only on input counts of 1 (i.e. when $A = 0$, $B = 0$, and $C = 1$) and 3 (when $A = 0$, $B = 1$, and $C = 1$). Implement the circuit with the fewest logic gates. Label the standard gates in your circuit drawing.

Q-13. Which input of the active-low latch must be activated to put the latch in the SET state?

Q-14. What logic levels must be applied to the inputs of the active-low latch to put it in the CLEAR state?

Q-15. What state of operation is the active-high latch in when both inputs are activated?