A Derived Physically Expressive Circuit Model for Multilayer RF Embedded Passives

Jie Wang and Ke-Li Wu, *Senior Member, IEEE*

***Abstract*—In this paper, a derived physically expressive circuit model is presented for automatically deriving an equivalent-circuit model of a multilayered embedded RF passive. The scheme is based on the partial-element equivalent-circuit (PEEC) model and a simple circuit transformation. By defining an appropriate cutoff criterion that is related to the highest frequency of interest, most of the internal nodes in the coupling circuit generated by the PEEC model can be approximately absorbed by the remaining frequency-independent *LC* elements progressively. The model is very simple to implement and has apparent physical meaning. Mathematically, this model progressively recombines the least significant system pole with other less significant poles. The resultant physically expressive circuit model will be very useful in designing multilayer embedded RF circuits. Four examples are given for demonstrating the validity and effectiveness of the scheme.**

***Index Terms*—Electromagnetic (EM) simulation, equivalent circuits, low-temperature co-fired ceramic (LTCC), RF circuits, system-on-package (SoP).**

I. Introduction

WITH THE fast development of low-loss and high-density integrated packaging technologies such as low-temperature co-fired ceramic (LTCC) [1], [2], system-on-package (SoP) [3] is considered as one of the most promising solutions for integrated electronic systems and wireless products. In designing an advanced SoP, one of the desired computer-aided design (CAD) tools is an algorithm that can systematically generate a physically meaningful circuit model for large-scale embedded RF passives and interconnection traces.

The needs for such a tool mainly comes from two aspects, which are: 1) a co-simulation of a mixed-signal heterogeneous system that consists of digital circuits, which are modeled by a circuit simulator in the time domain, and analog passive circuits, which are simulated by electromagnetic (EM) simulation in the frequency domain and 2) the prediction of electromagnetic interference (EMI) among the RF passive circuits. Although tremendous research has been done in EM modeling and the extraction of a circuit representation of embedded passives at gigahertz frequencies, the resultant circuit models are either limited to a predefined layout or the complexity of the models is overwhelming even with certain model simplification. Obviously, it is highly desirable to develop a systematic technique that can directly convert a generic layout of an RF embedded passive circuit to a concise circuit model that is valid in a given range of frequency. Preferably, the circuit model processes a clear physical meaning associated to the physical layout.

A number of techniques for extraction of lumped element equivalent circuits for embedded RF passives have been developed over the past years. The most popular technique is to construct an equivalent-circuit model based on a predefined circuit topology from physical intuition. The component values of the circuit model can be determined by empirical formulas or by curve fitting [4]. Due to the lack of good understanding of the parasitic coupling mechanism, for complex passive layouts, such a circuit model cannot be too sophisticated and unique. A systematic approach to extract a circuit model directly from EM simulation was proposed by Timmons and Wu in 2000 [5]. The approach is based on Cauer networks synthesis and the matching of the system poles and related residues instead of physical attributes. Although this approach is applicable to a sufficient wide frequency band of interest, the model can only supplant the original distributed RF circuit from the viewpoint of scattering parameters.

It is well known that the partial element equivalent circuit (PEEC) model is evolved from the mixed potential integral equation (MPIE). Under the quasi-static assumption, which can be readily justified for embedded RF passives whose dimension is much smaller than the wavelength, the PEEC model can generate a frequency-independent circuit model containing all self and mutual capacitance and inductance among all the discrete computational mesh elements of a multilayered circuit [6], [7]. Although the PEEC model, which will be called a coupling circuit model in this paper, can be regarded as a primitive equivalent circuit, the number of the circuit elements is excessive to handle for practical cases and the capacitors and inductors in the model do not have apparent physical meanings.

In this paper, a new methodology, called the derived physically expressive circuit model (DPECM), for systematically *deriving* an equivalent-circuit model for embedded multilayered RF passive circuits is presented. The method starts with the coupling circuit generated from the lossless quasi-static PEEC model and consists of a sequence of combining and deducting operations of a "Y-circuit" to a "Δ-circuit" on all the nodes of the coupling circuit model one by one. The method deletes each removable internal node in a coupling circuit model by first absorbing its fundamental attribute by its neighboring nodes and then omitting its minor attribute, which usually contributes only to the high-frequency response. Physically, the remaining internal nodes and the associated *LC* components in the resultant

Manuscript received December 2, 2005; revised February 18, 2006. This work was supported by the Innovation and Technology Fund and Research Grants Council Direct Research Grant of Hong Kong, Special Administrative Region, under Grant 6901523/ITS/011/03 and Grant 2050326.

The authors are with the Department of Electronic Engineering, The Chinese University of Hong Kong, Shatin, Hong Kong (e-mail: jwang@ee.cuhk.edu.hk; klwu@ee.cuhk.edu.hk).

Digital Object Identifier 10.1109/TMTT.2006.873621

circuit will dominate the main property of the original coupling circuit model and will present a clear physical meaning. Mathematically, the procedure is a model order reduction (MOR) [8]–[11] scheme. This is because each node combination and deduction operation performs the function of combining the effect of the least important poles with that of the other less important poles of the original coupling circuit model. This property will be illustrated by an example.

Thanks to its clear physical meaning, the circuit model derived by this scheme has been successfully applied to optimization designs of various LTCC embedded RF circuits [12] as a dynamic coarse model in the aggressive space mapping (ASM) [13].

II. Theory

A. PEEC Model

The PEEC algorithm was originally developed by Ruehli for modeling three-dimensional (3-D) multiconductor systems based on an integral-equation description of the geometry that is interpreted in terms of circuit elements. Since the structure under consideration is assumed to be very small, as compared to the wavelength, the quasi-static condition can be applied. In addition, the conductor loss and dielectric loss are omitted in this study for simplicity. The two major equations for building the coupling circuit of the PEEC model are

$$Lp_{mn} = \frac{\mu}{4\pi}\frac{1}{l_m l_n}\iint G_A(\vec{r},\vec{r}')dsds' \tag{1}$$

$$ps_{ij} = \frac{1}{4\pi\varepsilon}\frac{1}{s_i s_j}\iint G_\phi(\vec{r},\vec{r}')dsds' \tag{2}$$

where l_m and l_n are the lengths of inductive elements, S_i and S_j are areas of capacitive elements, and Lp and ps are partial inductance and coefficient of potential of the coupling circuit model, respectively. Notice that the integrals in the above equations are surface integrals for an infinite thin conducting strip model. A PEEC model concerning multilayered RF circuits with finite metal thickness has been developed in [14]. The static Green functions G_A and G_ϕ can be expressed in a series form as the kernel for the integrals.

As an example of PEEC modeling, Fig. 1(a) shows a group of typical computational mesh elements used in a PEEC model for modeling a short section of an infinitely thin straight conducting strip in which the capacitive meshes are represented by solid lines and the inductive meshes are represented by dash lines. Fig. 1(b) shows the corresponding PEEC coupling circuit model. It is seen that a capacitive mesh can be represented as a node and an inductive mesh is represented by an inductor between two nodes in the corresponding circuit. Once the meshes are generated and the nodes are identified, (1) and (2) are then applied on each pair of infinite thin inductive and capacitive meshes, respectively, to calculate the partial mutual inductance and coupling capacitance.

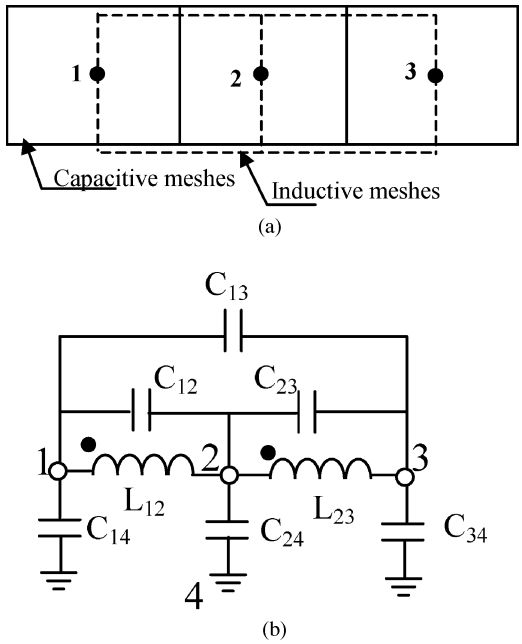


Fig. 1. (a) Inductive and capacitive meshes of a PEEC model. (b) Coupling circuit of the PEEC model.

B. Frequency-Dependent MOR

Once the general PEEC model converts the original 3-D multilayered embedded passive into a coupling circuit model, one can obtain its electric behavior by simulating the circuit using a circuit simulator. One of the methods for simulating the coupling circuit is the nodal voltage method, which will serve as the starting point of the MOR method to be presented in this paper. If the numbers of the external ports and the internal nodes in the circuit are N_{port} and N_{in}, respectively, the nodal voltage equation of the coupling circuit can be expressed as follows:

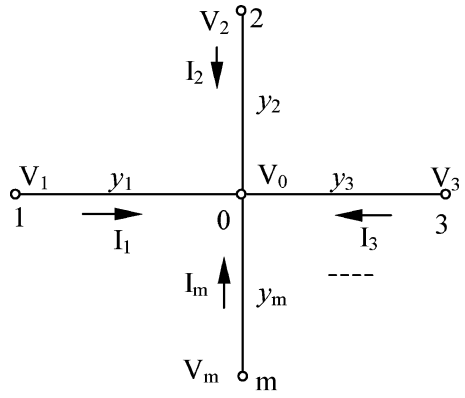
$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}\begin{bmatrix} V_{\text{in}} \\ V_{\text{port}} \end{bmatrix} = \begin{bmatrix} 0 \\ I \end{bmatrix}. \tag{3}$$

By the definition of the admittance matrix associated with external ports, the Y-parameters associated to the external ports can be found by

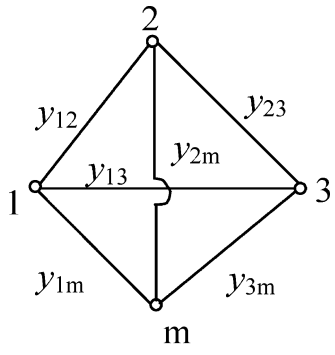
$$Y = Y_{22} - Y_{21}Y_{11}^{-1}Y_{12}. \tag{4}$$

Obviously, the computational expense of this expression for the Y-parameters of the circuit is proportional to N_{in}^3. To reduce the computational cost, an efficient way is to reduce the number of internal nodes of the coupling circuit model, i.e., to reduce the order of the matrix Y_{11} in (4).

The technique for reducing the number of nodes of the coupling circuit model is based on the conversion of a Y-circuit to a Δ-circuit. As shown in Fig. 2(a), node 0 that is to be deleted is connected to node i $(i = 1, 2, \ldots, m)$ through admittance y_i, which is the function of frequency. Assume the voltage at node



(a)



(b)

Fig. 2. (a) Y-circuit before node 0 is deleted. (b) Δ-circuit after node 0 is deleted.

i is V_i and the current in branch j is I_j, the following equations can be achieved by circuit theory:

$$\begin{cases} I_1 = y_1(V_1 - V_0) \\ I_2 = y_2(V_2 - V_0) \\ \cdots \\ I_m = y_m(V_m - V_0). \end{cases} \tag{5}$$

Since

$$I_1 + I_2 + \cdots + I_m = 0$$

there is

$$V_0 = \frac{y_1}{y_t}V_1 + \frac{y_2}{y_t}V_2 + \cdots + \frac{y_m}{y_t}V_m \tag{6}$$

where

$$y_t = y_1 + y_2 + \cdots y_m.$$

Substituting (6) into (5), we have

$$\begin{cases} I_1 = \dfrac{y_1y_2}{y_t}(V_1 - V_2) + \dfrac{y_1y_3}{y_t}(V_1 - V_3) + \cdots \\ \quad + \dfrac{y_1y_m}{y_t}(V_1 - V_m) \\ I_2 = \dfrac{y_2y_1}{y_t}(V_2 - V_1) + \dfrac{y_2y_3}{y_t}(V_2 - V_3) + \cdots \\ \quad + \dfrac{y_2y_m}{y_t}(V_2 - V_m) \\ \vdots \\ I_m = \dfrac{y_my_1}{y_t}(V_m - V_1) + \dfrac{y_my_2}{y_t}(V_m - V_2) + \cdots \\ \quad + \dfrac{y_my_{m-1}}{y_t}(V_m - V_{m-1}). \end{cases} \tag{7}$$

Equation (7) states that the Y-circuit is converted to a Δ-circuit shown in Fig. 2(b) after node 0 is deleted. The value y_{ij} in Fig. 2(b) can be expressed as

$$y_{ij} = \frac{y_iy_j}{y_t}. \tag{8}$$

Since y_i $(i = 1, 2, \ldots, m)$ is frequency dependent, y_{ij} will be a function of frequency. Nevertheless, all of the nodes, except the port nodes and ground nodes, can be deleted by this procedure node by node. It is worth mentioning that although this node deduction procedure is frequency dependent, it is still approximately ten times faster than evaluating (4) because there is no matrix inverse involved.

C. Frequency-Independent MOR

Since the above-mentioned MOR method is frequency dependent, the procedure must be repeated for every frequency sampling over a frequency range of interest. The fact suggests that if one can convert the coupling circuit model into a simpler circuit model by removing most of the internal nodes frequency independently with an acceptable approximation, not only does the order reduction need not be repeated for other frequencies, but the resultant circuit model may also incorporate certain physical meanings. To achieve the objective, let us discuss the frequency-independent MOR method.

We start with investigating the expression of y_{ij} in (8). Generally, y_i can be expressed as

$$y_i = j\varpi C_i + \frac{1}{j\varpi L_i}. \tag{9}$$

The admittance y_i can be expressed by (9) essentially because only the capacitor, inductor, and their combination tank are to be considered here. Thus, we can express y_{ij} as a function of frequency

$$y_{ij} = \frac{(j\varpi C_i + 1/j\varpi L_i)(j\varpi C_j + 1/j\varpi L_j)}{j\varpi C_t + 1/j\varpi L_t} \tag{10}$$

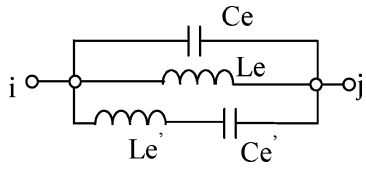


Fig. 3. Equivalent circuit for y_{ij}.

which can be further simplified as

$$y_{ij} = j\varpi C_e + \frac{1}{j\varpi L_e} + \frac{1}{j\varpi L'_e + 1/j\varpi C'_e} \tag{11}$$

where

$$\begin{aligned} C_e &= \frac{C_i C_j}{C_t} \\ L_e &= \frac{L_i L_j}{L_t} \\ L'_e &= \frac{C_t}{\alpha} \\ C'_e &= L_t \alpha \\ \alpha &= \frac{C_i}{L_j} + \frac{C_j}{L_i} - \frac{C_i C_j}{L_t C_t} - \frac{L_t C_t}{L_i L_j} \end{aligned} \tag{12}$$

where L_t and C_t are the total inductance and capacitance connected to the node to be deleted.

Obviously, y_{ij} can be interpreted by the equivalent circuit shown in Fig. 3.

Each component in this circuit is frequency independent. Although the circuit shown in Fig. 3 is a representation of (11) without any approximation, it is not suitable for further manipulation because the series of capacitor C'_e and inductor L'_e brings some frequency-dependent terms in deleting node i or node j in the subsequent steps. When (11) for y_{ij} is used in the next steps for deleting node i or j, the resultant combined branch admittance will not have the same simple format as that in (9) any more. In order to derive a frequency-independent circuit mode, some approximation needs to be done to simplify the third term of (11)

$$y_{ij}^{(3)} = \frac{1}{j\varpi L'_e + 1/j\varpi C'_e} = \frac{j\varpi C'_e}{1 - \varpi^2 L'_e C'_e} = \frac{j\varpi C'_e}{1 - \varpi^2 L_t C_t}. \tag{13}$$

If $\varpi^2 L_t C_t \ll 1$,

$$y_{ij}^{(3)} \approx \frac{j\varpi C'_e}{1 - \varpi_0^2 L_t C_t}$$

where $\varpi_0 = \sqrt{\sum_{n=1}^{N} \varpi_n^2 / N}$ is chosen to minimize an average error in the given frequency range of interest, N is the number of frequency samples, and ϖ_n is the angular frequency of the nth frequency sample. This approximation means that a capacitor is used to replace the original *LC* serial resonator. This approximation is acceptable when the resonance frequency of the resonator is much higher than a cutoff frequency of interest.

Having had the approximation, (12) will be rewritten as

$$y_{ij} = j\varpi C''_e + 1/j\varpi L_e \tag{14}$$

where

$$C''_e = \frac{C_i C_j}{C_t} + \frac{\alpha L_t}{1 - \varpi_0^2 L_t C_t} \quad L_e = \frac{L_i L_j}{L_t}.$$

Therefore, if an internal node of a coupling circuit model satisfies the condition of $\varpi^2 L_t C_t \ll 1$, it is called a removable node. Note that (14) combines the major influence of the removable node into those nodes that are immediately connected to the node. The condition of $\varpi^2 L_t C_t \ll 1$ means that the interaction between the capacitive and inductive couplings associated to an internal node is very weak over the frequency range of interest. For a coupling circuit model generated from the PEEC, most of the coupling capacitances and inductances are usually small enough. Therefore, the condition is true for most of the internal nodes for the frequencies in the gigahertz range.

To show that the procedure described above can lead to a physically expressive circuit model, we take the coupling circuit model in Fig. 1(b) as an example. At low frequencies, the current flowing through the inductors of L_{12} and L_{23} (L_{12} means the inductor between nodes 1 and 2) has almost the same value due to the small shunt capacitance of C_{12}, C_{23}, and C_{24}, where subscript 4 denotes the ground node. Due to this physical phenomenon, we can delete node 2 by combining the two inductors into one whose value is equal to $L_{12}L_{23}/(L_{12} + L_{23})$ according to (14). The shunt capacitors of C_{12}, C_{23}, and C_{24} will be combined to C_{14}, C_{34}, and C_{13} with their values determined by (14). At this stage, the number of meshes shown in Fig. 1(a) is reduced from 3 to 2. Node 1 and 3 will represent nodes with larger areas and their shunt capacitances to ground will increase. The increased capacitance and inductance associated with nodes 1 and 3 may not satisfy the approximate condition at nodes 1 and 3. If this is the case, the nodes will be left in the ultimate equivalent circuit; otherwise, the nodes will be deleted by the "combing-and-deducting" process. It can be seen that this procedure retains the essential attribute at each local feature (node) and eliminates the insignificant effects associated to the local feature. The significant local attributes are then consolidated by a few more prominent circuit elements, which have clearer physical meanings. For a complex 3-D multilayered structure, the same node deduction procedure can be systematically applied to each internal node in the coupling circuit model. The nodes that do not satisfy the approximate condition will be retained to form the final equivalent-circuit model.

To implement the MOR procedure with a high degree of fidelity, the following two important details should be discussed.

1) In a practical implementation, we can set a cutoff value δ for gauging every node by its value of $\varpi^2 L_t C_t$ throughout an entire coupling circuit model. It means that if a node satisfies

$$\varpi_{\max}^2 L_t C_t < \delta \tag{15}$$

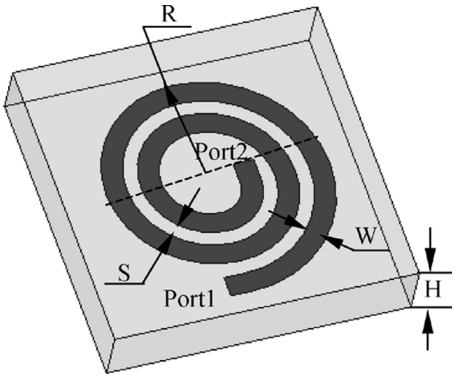


Fig. 4. Circular spiral inductor.

where $\varpi_{\max}$ is the highest angular frequency of interest, it will be considered as a removable node. The smaller the value δ is, the more nodes will be retained in the final equivalent circuit. In the examples throughout this paper, the cutoff value δ is set to 0.15.

2) Since the coupling circuit model will be a dynamic circuit during the MOR iteration, one must select a judicious pattern for reducing the number of internal nodes. It is found that by removing the most removable node, whose $\varpi_{\max}^2 L_t C_t$ is the least among all the remaining internal nodes, at each step of the iteration the process can retain the essential attribute of the circuit most. This is because the node with least $\varpi_{\max}^2 L_t C_t$ corresponds to the least important pole of the original system. This point will be illustrated by an example in Section III.

The benefits of having a frequency-independent and model order reduced circuit model are obvious. First, the circuit model reveals a clear correlation between the circuit mode and the physical circuit layout. The circuit model consists of not only the elements of major capacitance and inductance, but also the components exhibiting the higher order parasitic couplings. Second, since the order of the original coupling circuit model has been significantly reduced, and the MOR process only needs to be done once, the simulation expense will be greatly reduced even when the time for the MOR is counted.

III. Application Examples

The examples presented here are typical embedded RF passives in LTCC SoP modules. All of the full-wave EM simulation results are obtained by using CST Microwave Studio (V.5.1.3).

The first example is a planar circular spiral inductor, as illustrated in Fig. 4. The inductor is located at height of h in a grounded substrate whose height is H. The dimensions of the inductor are $R = 0.85$, $W = 0.15$, $S = 0.1$, $h = 0.239$, and $H = 0.437$ (all in millimeters). The dielectric constant of the substrate is 9.1. The original coupling circuit model generated from the PEEC model has 16 internal nodes. After a MOR process, only one internal node is left. The corresponding derived lumped-element circuit model is shown in Fig. 5(a). The physical meaning of each component of the circuit model is obvious. The inductors L_{12} and L_{31} in this equivalent-circuit model denote the main partial inductance that we want to achieve and the capacitors C_{14}, C_{24}, and C_{34} (4 is the ground node) are due to the parasite effects between the strip and ground. Due to the shunt parasitic capacitor, this inductor is divided into two parts with a mutual inductive coupling M. The S-parameters of the two-port structure computed by a full-wave EM model and the derived circuit model are presented in Fig. 6. Good agreement can be observed.

The equivalent circuit of this inductor can be further simplified into a model with only one inductor and two shunt parasitic capacitors if the accuracy is not the first priority. The simpler

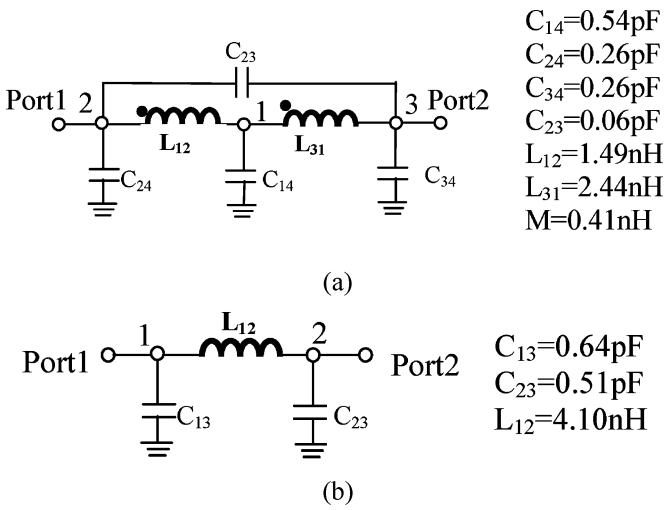


Fig. 5. Equivalent circuit of the circular spiral inductor.

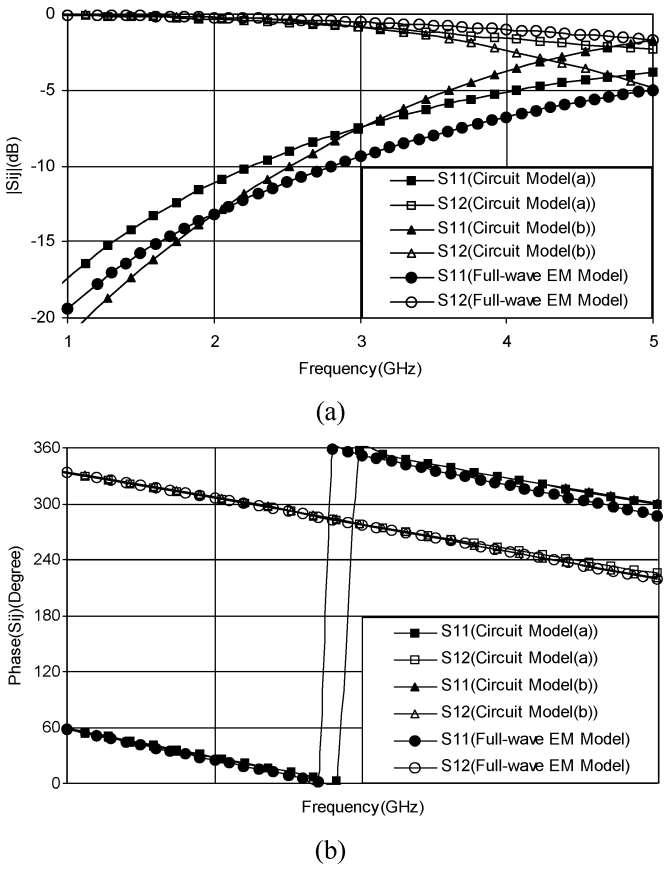


Fig. 6. S-parameters of: (a) magnitude and (b) phase of the derived equivalent circuits and full-wave EM model for the circular spiral inductor.

TABLE I
SYSTEM POLES OF Y-MATRIX FOR THE SPIRAL INDUCTOR IN THE DPECM PROCESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
8.05	8.05	8.05	8.05	8.05	8.05	8.06	8.07	8.08	8.10	8.10	8.10	8.20	8.20	8.26	8.69
12.63	12.63	12.64	12.65	12.68	12.72	12.72	12.78	12.83	12.95	12.96	13.15	13.24	13.69	16.49	
19.31	19.31	19.43	19.45	19.54	19.55	19.66	19.75	19.79	19.80	20.20	20.74	21.85	23.83		
25.25	25.34	25.46	25.47	25.62	25.64	25.67	25.67	25.92	26.25	27.67	28.33	28.64			
31.15	31.20	31.27	31.35	31.65	32.07	32.55	32.90	32.91	34.43	35.28	37.53				
34.60	34.64	34.84	35.14	35.14	35.77	36.04	36.75	37.32	37.34	38.08					
40.54	40.59	40.66	40.80	40.85	40.87	41.78	42.94	44.58	45.17						
45.61	45.71	45.72	46.08	46.28	46.57	47.50	47.60	48.16							
49.27	49.52	49.56	50.37	51.27	51.91	52.01	52.46								
52.26	52.92	53.12	53.82	55.51	56.30	56.34									
54.81	55.42	56.21	56.35	56.64	59.08										
58.29	58.29	58.32	59.60	61.21											
61.13	61.23	61.25	63.09												
63.84	65.00	65.01													
65.03	67.53														
71.38															

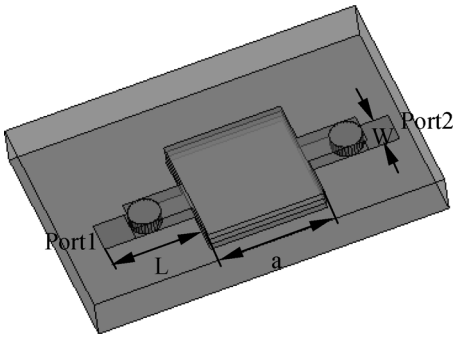


Fig. 7. Four-layer capacitor.

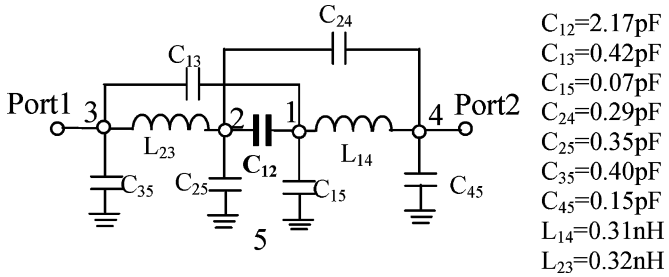


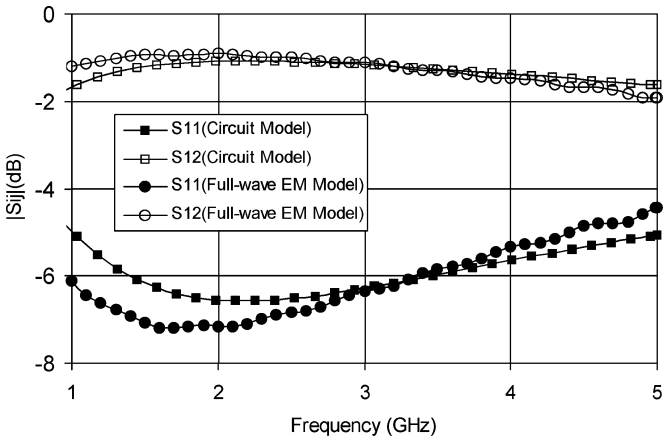
Fig. 8. Derived equivalent circuit of the four-layer capacitor.

circuit model is shown in Fig. 5(b) and the corresponding S-parameters are superposed in Fig. 6. In this case, the cutoff value δ is set to 0.65. The S-parameter comparison of the circuit models [see Fig. 6(a) and (b)] and the full-wave EM model shown in Fig. 6 indicates that the circuit model [see Fig. 6(a)] is more accurate than the circuit model [see Fig. 6(b)].

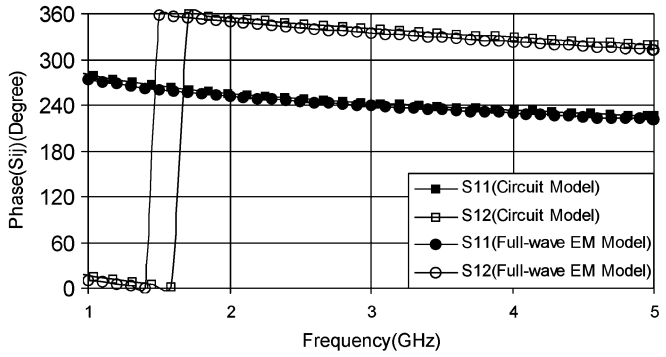
In order to mathematically justify the proposed MOR scheme presented in this paper, the system poles of the Y-matrix for this spiral inductor circuit can be found using the modified nodal analysis (MNA) method [15]. The system poles of the Y-matrix after each internal removable node being removed are listed in Table I. The first row in this table represents the number of internal nodes that have been deleted. The columns list the corresponding system poles, in the order of descending importance, that exist in pairs symmetric to the origin. Interestingly, from this table, one can find that after each node is removed, the largest pole, i.e., the least important pole, is "absorbed" by other less significant poles.

The second example is a four-layer capacitor that is embedded in a substrate with a height of $H = 0.274$ mm, as shown in Fig. 7. The four square plates with heights of $h1 = 0.091$, $h2 = 0.137$, $h3 = 0.182$, and $h4 = 0.228$ (all in millimeters) have the same dimension of $a \times a = 0.762$ mm $\times$ 0.762 mm. The dimension of the input/output strip is $L \times W = 0.254$ mm $\times$ 0.100 mm. The dielectric constant of the substrate is 7.8. The equivalent circuit of this four-layer structure is derived as shown in Fig. 8. In this circuit, node 1 denotes the two plates connected by the via-hole from layers 1 to 3; node 2 corresponds to the two plates in layers 2 and 3 that are also connected by a via-hole; nodes 3 and 4 denote the two ports; and node 5 is the ground node. Each component in this circuit has an obvious physically meaning associated to the original layout. The capacitor between nodes 1 and 2 is the main capacitor of interest. The capacitors between nodes 1–5 are introduced because of the parasite effects between the plates and ground. The discontinuities between the input/output strips and the square plates lead to the two parasitic inductors L_{23} and L_{14} in the circuit model, and capacitors C_{13} and C_{24} are parasitic capacitors. The S-parameters by the full-wave EM model and the derived equivalent circuit are shown in Fig. 9 and agreement is excellent.

The third example is a multilayer high-pass filter, as shown in Fig. 10. The filter is constructed by an eight-layer substrate with a dielectric constant of 9.1 and a thinnest tape thickness of 0.041 mm. The thickness of the conductor is 0.01 mm. In other words, the metallization thickness is approximately one-fourth of the thinnest dielectric thickness. In order to accurately model this filter whose metallization thickness cannot be neglected, a novel PEEC algorithm without increasing the number of PEEC circuit elements is applied for generating the coupling circuit model [14]. The proposed DPECM is then used to derive the equivalent circuit, which is depicted in Fig. 11. Note that L_{23}, L_{14}, C_{24}, C_{45}, and C_{15} are the main elements of the original high-pass filter schematic and C_{23}, C_{14}, C_{35}, and C_{45} are parasitic elements. The S-parameters of the equivalent circuit and the full-wave EM simulation are superposed in Fig. 12 and good



(a)



(b)

Fig. 9. S-parameters of: (a) magnitude and (b) phase of the derived equivalent circuit and full-wave EM model for the four-layer capacitor.

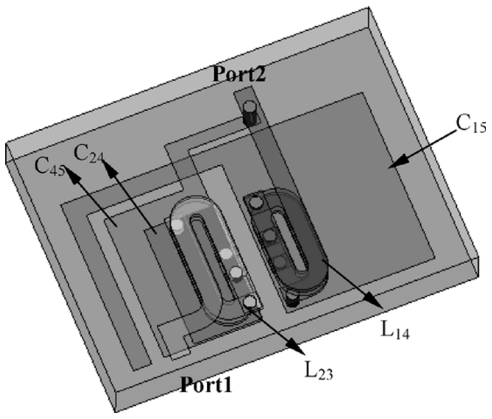


Fig. 10. High-pass filter.

agreement can also be observed. The time for DPECM is approximately 10 s, while the time for the full-wave EM simulation by CST is approximately 1200 s.

The fourth example is a multilayer bandpass filter, as shown in Fig. 13. The filter is constructed by a seven-layer substrate with dielectric constant of 7.8 and a thinnest tape thickness of 0.043 mm. The thickness of the conductor is 0.01 mm. The derived equivalent circuit of this bandpass filter is shown in Fig. 14. Note that L_{17}, L_{27}, L_{35}, L_{46}, C_{13}, C_{17}, C_{24}, C_{27}, and C_{34} are the main elements of the original bandpass filter

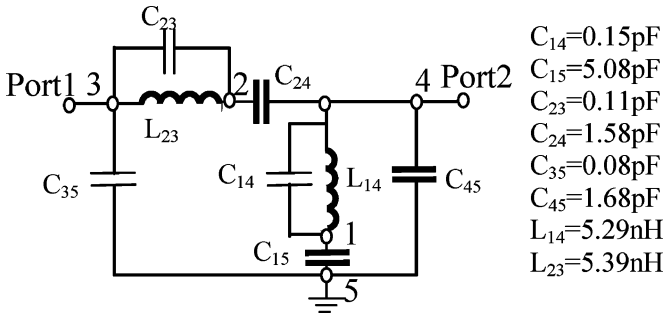


Fig. 11. Derived equivalent circuit of the high-pass filter.

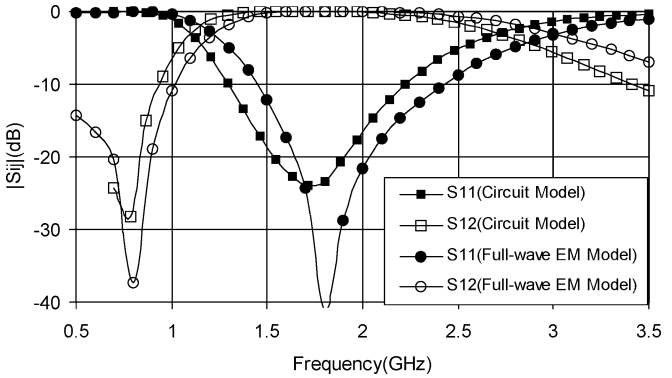


Fig. 12. S-parameters of the equivalent circuit and full-wave EM model for the high-pass filter.

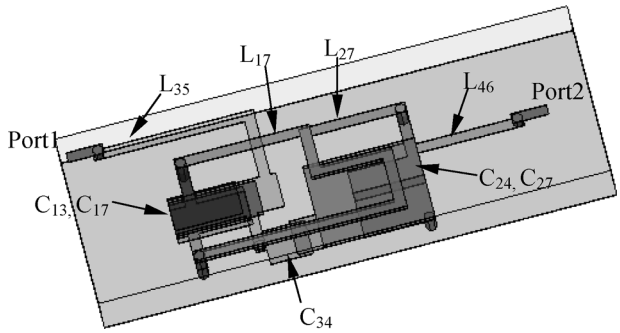


Fig. 13. Bandpass filter.

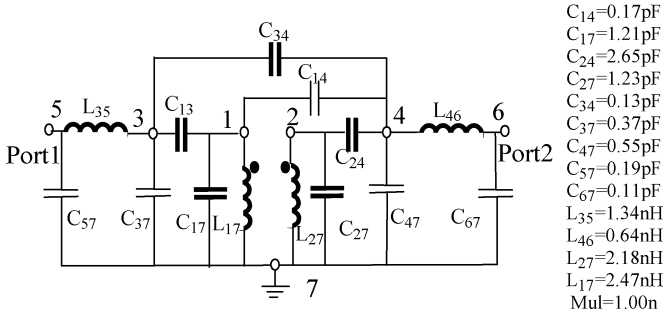


Fig. 14. Derived equivalent circuit of the bandpass filter.

schematic and others are parasitic elements. This bandpass filter has been built using LTCC technology. The S-parameters of the equivalent circuit and the measurement, as well as full-wave EM model, are superposed in Fig. 15, and good agreement can also

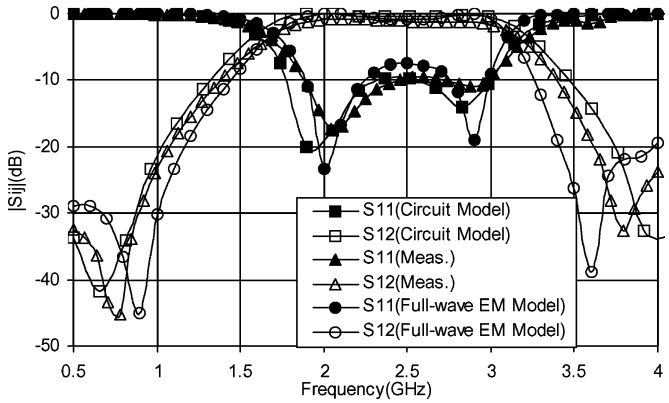


Fig. 15. S-parameters of the equivalent circuit, measurement, and the full-wave EM model for the bandpass filter.

be observed. The time for the DPECM and then to perform a simulation is approximately 7 s, while the time for the full-wave EM simulation by CST is approximately 280 s.

IV. Conclusion

A novel DPECM for embedded RF passives has been presented. The model is based on a quasi-static PEEC model and a simple systematic MOR scheme. Due to the quasi-static natural of the PEEC model, this DPECM is accurate enough for RF embedded passives when the frequency of interest is lower than 5.0 GHz. The circuit model has been proven to be effective and robust in deriving a physically expressive equivalent circuit of a 3-D multilayer RF passive circuit without any physical intuition and prior knowledge. Since the computation time for deriving the circuit model and generating the S-parameters over a wide frequency band of interest is a few orders of magnitude faster than any full-wave EM simulator, the proposed scheme can be used as a real time design library for embedded RF passives.

Four examples have been provided to illustrate the details and effectiveness of the model. Since each component in the equivalent circuit obviously relates to a part of the original layout, one can physically adjust the dimension of the structure in order to achieve the desired values of the components of interest when designing an embedded RF circuit. The equivalent-circuit model can be extended to the cases with substrate loss and conductor loss. For high-frequency applications, a full-wave Green's function for layered media should be used to accommodate the radiation loss. All these extensions of the proposed model will be reported in future work.

References

[1] A. Sutono, D. Heo, Y.-J. E. Chen, and J. Laskar, "High-Q LTCC based passive library for wireless system-on-package (SOP) module development," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 10, pp. 1715–1724, Oct. 2001.

[2] K. Rambabu and J. Bornemann, "Simplified analysis technique for the initial design of LTCC filters with all-capacitive coupling," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 5, pp. 1787–1791, May 2005.

[3] K. Lim *et al.*, "RF-system-on-package (SOP) for wireless communications," *IEEE Micro*, vol. 3, no. 1, pp. 88–99, Mar. 2002.

[4] P. L. Werner, R. Mittra, and D. H. Werner, "Extraction of SPICE-type equivalent circuits of microwave components and discontinuities using the genetic algorithm optimization technique," *IEEE Trans. Compon., Packag., Manuf. Technol. B*, vol. 23, no. 1, pp. 55–61, Feb. 2000.

[5] I. Timmins and K.-L. Wu, "An efficient systematic approach to model extraction for passive microwave circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1565–1573, Sep. 2000.

[6] A. E. Ruehli, "Equivalent circuit models for three-dimensional multi-conductor systems," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, no. 3, pp. 216–221, Mar. 1974.

[7] H. Heeb and A. E. Ruehli, "Three-dimensional interconnect analysis using partial element equivalent circuits," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 39, no. 11, pp. 974–982, Nov. 1992.

[8] N. Marques, M. Kamon, J. White, and L. M. Silvera, "A mixed nodal-mesh formulation for efficient extraction and passive reduced-order modeling of 3-D interconnects," in *Proc. Design Autom. Conf.*, San Francisco, CA, Jun. 1998, vol. 35, pp. 297–302.

[9] A. Odabasioglu, M. Celik, and L. T. Plieggi, "PRIMA: Passive reduced-order internnect macromodeling algorithm," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 17, no. 8, pp. 645–654, Aug. 1998.

[10] A. C. Cangellaris and M. Igarashi, "Rules for robust generation of accurate reduced-order models of high-speed coupled interconnections," in *50th Electron. Compon. Technol. Conf.*, Las Vegas, NV, May 2000, pp. 502–507.

[11] J. Cullum, A. Ruehli, and T. Zhang, "A method for reduced-order modeling and simulation of large interconnect circuits and its application to PEEC models with retardation," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.*, vol. 47, no. 4, pp. 261–273, Apr. 2000.

[12] K.-L. Wu, Y.-J. Zhao, J. Wang, and M. K. K. Cheng, "An effective dynamic coarse model for optimization design of LTCC RF circuits with aggressive space mapping," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, pp. 393–402, Jan. 2004.

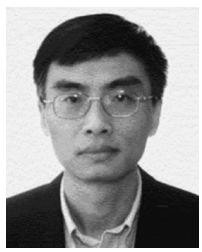
[13] J. W. Bandler, R. M. Biernacki, S. H. Chen, R. H. Hemmers, and K. Madsen, "Electromagnetic optimization exploiting aggressive space mapping," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 12, pp. 2874–2882, Dec. 1995.

[14] K. L. Wu, L. K. Yeung, and Y. Ding, "An efficient PEEC algorithm for modeling of LTCC RF circuits with finite metal strip thickness," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 9, pp. 390–392, Sep. 2003.

[15] C.-W. Ho, A. E. Ruehli, and P. A. Brennan, "The modified nodal approach to network analysis," *IEEE Trans. Circuits Syst.*, vol. CAS-22, no. 6, pp. 504–509, Jun. 1975.

Jie Wang was born in JiangSu Province, China, in 1975. He received the B.S. and Ph.D. degrees from the Southeast University of China, Nanjing, China, in 1996 and 2001, respectively, both in radio engineering.

Since January 2002, he has been with The Chinese University of Hong Kong, Shatin, Hong Kong, where he is currently a Post-Doctoral Fellow. His current research interests include the development of EM modeling for multilayer embedded RF passives and the design of various RF modules by using LTCC technology.



Ke-Li Wu (M'90–SM'96) received the B.S. and M.Eng degree from Nanjing University of Science and Technology, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Laval University, Quebec, QC, Canada, in 1989.

From 1989 to 1993, he was with the Communications Research Laboratory, McMaster University, as a Research Engineer. In March 1993, he joined the Corporate Research and Development Division, Com Dev International, Cambridge, ON, Canada, where he was a Principal Member of Technical Staff in charge of developing advanced EM design software for microwave subsystems for satellite and wireless communications. Since October 1999, he has been with the Department of Electronic Engineering, The Chinese University of Hong Kong, where he is currently a Professor. He has authored or coauthored numerous publications in the areas of EM modeling and microwave and antenna engineering. His current research interests include EM modeling, microwave filters, LTCC technology, multichip module (MCM) technologies, antennas for wireless terminals, and active RFID systems.