and verified both dual and single port functionality over the range −50°C to +50°C. Throughout this range a 0·8 V minimum supply setting can be maintained and an input logic low voltage limit of greater than 0·3 V is measured. Above +50°C the low voltage margin is found to drop sharply and thus prohibit device operation. Typical dual port speed and power characteristics over temperature are indicated in Fig. 4.
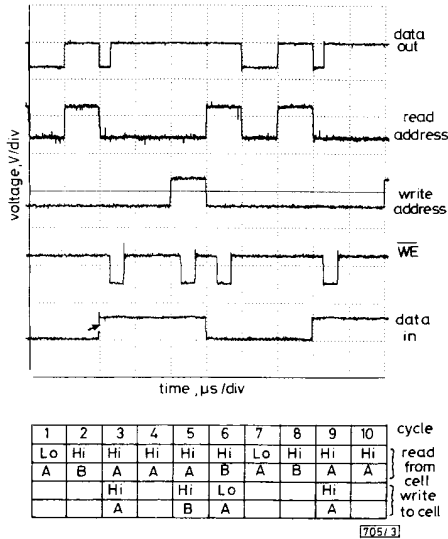

Fig. 3 *Oscilloscope waveforms demonstrating functional operations*

1	2	3	4	5	6	7	8	9	10	cycle
Lo	Hi	Hi	Hi	Hi	Hi	Lo	Hi	Hi	Hi	read from cell
A	B	A	A	A	B	A	B	A	A	
		Hi			Hi	Lo			Hi	write to cell
		A			B	A			A	

In TDM switch applications the 32 × 8 dual port can be used to store a data byte of one frame and simultaneously transmit a data byte of another. Since switch throughput is predominantly governed by register speed, the 32 × 8 dual port would be capable of supporting 32 channel frames at over 200 Mbyte/s total throughput (5 ns cycle time) or 6·25 Mbytes/s per channel at room temperature. This is contrasted with a switch implementation employing the 32 × 8 single port which again can operate at a 5 ns cycle time but achieve roughly half the throughput because of the need for separate store and transmit cycles.
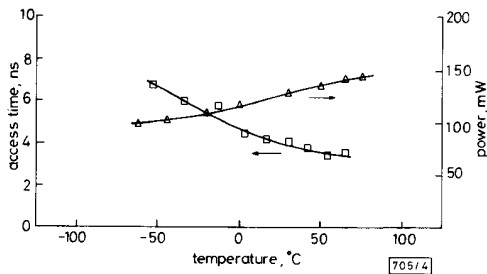

Fig. 4 *Access time and power dissipation of dual port array*

The results obtained demonstrate the feasibility of extending GaAs E/D MESFET digital logic technology to include SRAM register capability. Fully function high speed 32 × 8 dual and single port SRAM arrays have been achieved with 0·5 mW/bit to provide a near ten-fold improvement in dissipation over GaAs MESFET register blocks constructed using flip-flop circuitry.[6]

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BOUNDARY ELEMENT METHOD FOR MODELLING MIC DEVICES

Indexing terms: Modelling, Microwave techniques

A new model for analysing discontinuities in MIC devices is proposed. The technique is based on the boundary element method. An MIC device with an arbitrarily shaped discontinuity can be treated as a one-dimensional problem. Two numerical examples are given to check the validity of the model.

Obtaining the dynamic properties of MIC devices has required much effort. In particular, determining the properties of discontinuities and components in passive circuits has proved difficult. Activity has focussed on the use of the waveguide model, which usually consists of parallel plates of effective width W_{eff}, magnetic walls around the sides and a dielectric medium of effective relative permittivity ε_{eff}.[1-3] The dielectric medium fills the interior of the waveguide, i.e. the region contained by the electric and magnetic walls. Electromagnetic circuit modelling has developed the mode-matching method to solve MIC problems. The finite element method has also been used on the homogeneous discontinuity region. The main limitations to these techniques are that they can only be applied to discontinuities with simple geometries, and if the complexity of the discontinuities is increased, the computational overhead becomes excessively large. It should be noted that the planar waveguide model has a simplifying assumption. The dielectric within the waveguide is assumed totally homogeneous, or at least, that it consists of a collection of homogeneous regions. In this letter is is shown that the boundary element method (BEM) is well suited to solving MIC circuit properties. It has the advantage that it can be used to solve complex boundary geometries, as well as having a low computational overhead.

The device's equivalent waveguide circuit is divided into boundary elements as shown in Fig. 1 when applying the BEM to a device. The boundary element matrix equation can be written

$$[H_0, H_1, H_2, \ldots, H_M] \begin{bmatrix} \{E_z\}_{\Gamma_0} \\ \{E_z\}_{\Gamma_1} \\ \vdots \\ \{E_z\}_{\Gamma_M} \end{bmatrix}$$

$$= [G_0, G_1, G_2, \ldots, G_M] \begin{bmatrix} \{\partial E_z/\partial n\}_{\Gamma_0} \\ \{\partial E_z/\partial n\}_{\Gamma_1} \\ \vdots \\ \{\partial E_z/\partial n\}_{\Gamma_M} \end{bmatrix} \quad (1)$$

where Γ_i $(i = 1, 2, \ldots, M)$ is the boundary on the device ports, Γ_0 represents the magnetic wall boundary. $\{E_z\}_{\Gamma_i}$ and $\{\partial E_z/\partial n\}_{\Gamma_i}$ is the z-directed electrical field and its normal derivative on the boundary Γ_i, respectively. A detailed discussion of the sub-matrix H_i and G_i is given in Reference 4.
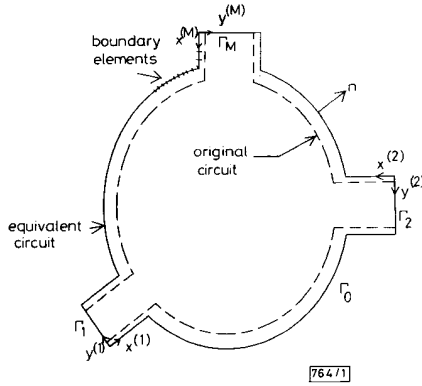

Fig. 1 *Geometry of MIC device and boundary elements*

Using the magnetic wall boundary condition and the analytical relation on the waveguide ports

$$E_z(x^{(i)} = 0, y^{(i)})\Big|_{\Gamma_i} = 2\delta_{ij} f_{i0}(y^{(i)})$$

$$- \sum_{m=0}^{\infty} \frac{1}{j\beta_{im}} \int_0^{W_i} f_{im}(y_0^{(i)}) f_{im}(y^{(i)}) \frac{\partial E_z}{\partial n}(y_0^{(i)})\Big|_{\Gamma_i} dy_0^{(i)} \quad (2)$$

where

$$f_{im} = \begin{cases} \sqrt{\left(\dfrac{2}{W_i}\right)} \cos\left(m\pi y/W_i\right) & m = 1, 2, \ldots \\ \sqrt{\left(\dfrac{1}{W_i}\right)} & m = 0 \end{cases} \quad (3)$$

$$\beta_{im} = \sqrt{[k_0^2 - (m\pi/W_i)^2]} \qquad m = 0, 1, 2, \ldots \quad (4)$$

Assuming a fundamental model wave incidents from port i and discretising eqn. 2, a final matrix equation can be obtained

$$\begin{bmatrix} H_0 & H_1 & \ldots & H_M & -G_1 & -G_2 & \ldots & -G_M \\ [0] & [1] & \ldots & [0] & -[Z_1] & [0] & \ldots & [0] \\ \vdots & \vdots & \ldots & \vdots & \vdots & \vdots & \ldots & \vdots \\ [0] & [0] & \ldots & [1] & [0] & [0] & \ldots & -[Z_M] \end{bmatrix}$$

$$\begin{Bmatrix} \{E_z\}_{\Gamma_0} \\ \{E_z\}_{\Gamma_1} \\ \vdots \\ \{E_z\}_{\Gamma_M} \\ \left\{\dfrac{\partial E_z}{\partial n}\right\}_{\Gamma_0} \\ \vdots \\ \left\{\dfrac{\partial E_z}{\partial n}\right\}_{\Gamma_M} \end{Bmatrix} = \begin{Bmatrix} 0 \\ \vdots \\ 0 \\ 2\delta_{ij} f_{i0} \\ 0 \\ \vdots \\ 0 \end{Bmatrix} \quad (5)$$

where

$$[Z_i] = -\sum_{m=0}^{\infty} \left(\frac{1}{j\beta_{im}}\right)\{f_{im}\} \sum_{e'} \int_{e'} f_{im}(y_0^{(i)})$$

$$\times N(x^{(i)} = 0, y_0^{(i)}) \, dy_0^{(i)} \qquad i = 1, 2, \ldots, M \quad (6)$$

The components of the $\{f_{im}\}$ vector are the values of $f_{im}(y^{(i)})$ at the nodal points on Γ_i, N is the shape function of boundary element, and $\sum_{e'}$ extends over the elements related to Γ_i.

Two numerical examples are discussed for the purpose of checking the model. Fig. 2b shows the transmission coefficient $|T_{12}|$ of a stripline band elimination filter. Its equivalent waveguide circuit configured with a suitable set of boundary elements, is shown in Fig. 2a. The agreement in Fig. 2b between the BEM and the finite element results, as well as the BEM and the experimental results is fairly good. The behaviour predicated by the boundary element method at the resonant frequency, agrees with that predicated by Reference 5. As an example of a microstrip MIC devices, a T-junction is studied.
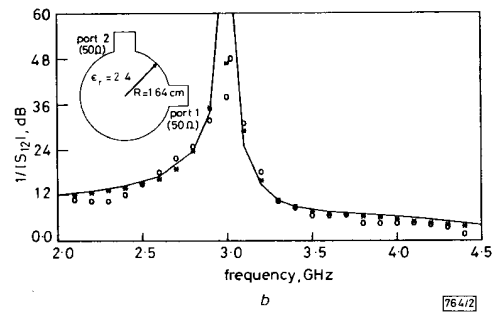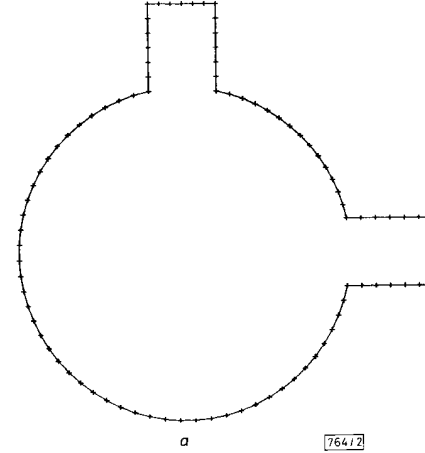

Fig. 2 *Stripline band elimination filter*

a Boundary element discretisation of the planar waveguide model
b Transmission coefficient

The numerical results of S-parameters calculations are shown in Fig. 3. The agreement with the finite element solution is satisfactory. For all the numerical examples discussed here, the power conservation condition is satisfied to an accuracy of $\pm 10^{-5}$ to $\pm 10^{-4}$.

In conclusion, we have proposed a new numerical model for analysing MIC devices. Generally speaking, the boundary element always reduces the dimension of the original problem
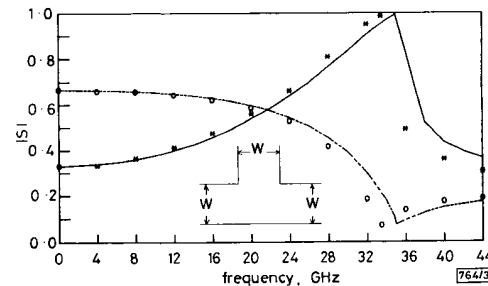

Fig. 3 *Reflection and transmission coefficients of T-junction*

by one. That is, the planar waveguide model of a MIC device, can be reduced from a two-dimensional problem to a one-dimensional problem. As a result, the planar waveguide model become easier to use and more efficient to run. A model for loaded MIC devices is currently under development at our laboratory. It uses the recently developed coupled finite-boundary element method.[6]

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SELF-ROUTING PLANAR NETWORK FOR GUIDED-WAVE OPTICAL SWITCHING SYSTEMS

Indexing terms: Optical switching, Self-routing, Planar network, Waveguides

An $N \times N$ self-routing planar network suitable for fabricating optical space switches on lithium niobate substrate is presented. The network has $O(N^2)$ cross points, good modularity and expandability. It also has no waveguide crossovers and no differential attenuation between any of the input and output pairs. A self-routing control can be applied to this network, which is indispensable for ATM switching systems.

Introduction: Although many switching networks are available in the electronics domain, optical architectures with a self-routing capability[1] are essential for the switching and cross-connection systems of future B-ISDN. Such architectures would have the properties of optical transparency and very high data-rate capacity, as well as distributed and fast control.

This letter describes a self-routing switching network for optical space switches based on lithium niobate cross points driven by their electrodes. There are some important requirements to take into consideration when designing this type of optical switch architecture. The number of switch elements and waveguide crossovers; and the attenuation are among these. A planar network architecture with $O(N^2)$ cross points that does not require waveguide crossovers has been proposed.[2,3]

Some planar networks are strictly nonblocking and it is easy to form connections between any of the input ports. Only a few planar architectures with self-routing capability are known.[4] This letter presents an $N \times N$ planar network with that capability. The self-routing algorithm and an example of its operation are also briefly described.

Self-routing planar network architecture: The target system architecture is shown in Fig. 1.[5] Fixed length packets are synchronously fed into the network. The header of a packet, including the designated output port number, is stripped off

and converted into an electrical signal at the input. The separated header is then processed in the electrical overlay network. The remaining packet data passes through the waveguides into the optical network. Each of the cross points is driven by their individual electrode, which is in turn activated by the control signal given by the corresponding processing element in the electrical overlay network, as shown in Fig. 1.
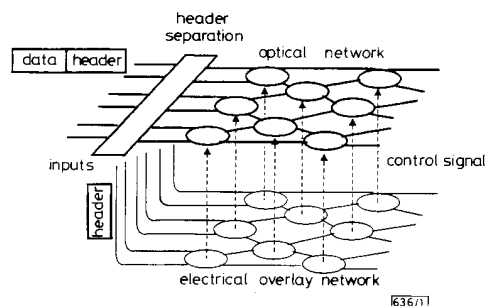

Fig. 1 Target system architecture

The proposed self-routing planar network architecture is shown in Fig. 2. Both the optical and electrical networks have the same construction as Fig. 2. A 2×2 switch element (i.e. a β element) has two possible states; cross and bar. The state of a β element in the electrical overlay network is decided by the combination of destination numbers fed into that element. The state of a β element in the optical network is determined by its corresponding β element in the electrical overlay network.
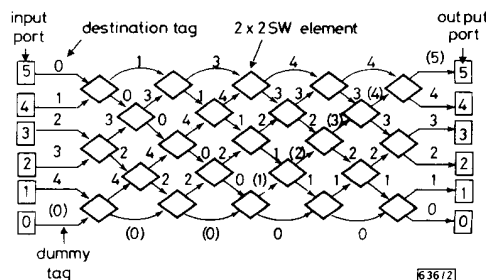

Fig. 2 Self-routing planar switch architecture

The proposed $N \times N$ non blocking network requires $2N - 3$ stages for an even number N. Fig. 2 is an example of a 6×6 switch construction. This network has no crossovers and no differential attenuation, if the highest and lowest numbered input ports are not used. Such characteristics allow dense fabrications of the cross points, low cross talk between the waveguides, and the easy design of optical receivers.

Self-routing control: Operation of a β element in the electrical plane can be described as follows. A destination number in each packet is stripped off at the input ports. If thee is no packet to send, add a dummy tag that includes the input port number and a dummy flag. The flag is represented by brackets in Fig. 2 and Fig. 3. For example, no packet has arrived at input port 0 in Fig. 2, so a dummy tag, (0), is given at the input port.

Let N_u and N_d be the destination numbers for packets at the upper and lower input links of a β element as shown in Fig. 3. The β element is set in the cross state if N_u is smaller than or equal to N_d; this is also true for dummy flags. Note that a destination number with a dummy flag (i.e. bracketed number) increases or decreases by one, according to its input link position, as shown in Fig. 3a. Set the β element in the bar state if N_u is greater than N_d as shown in Fig. 3b.

The packet flow for a required connection is shown in Fig. 2. All the numbers depicted in Fig. 2 represent destination tags and the bracketed numbers represent dummy tags. Let us follow the destination tag at input port 5. That tag is designated for output port 0. From the first to the fifth stage, the