

# An I/O Coupling Multiplier Circuit and Its Application to Wideband Filters and Diplexers

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**Abstract**—In this paper, a novel input/output (I/O) coupling multiplier circuit for conveniently increasing I/O coupling of a wideband coupled-resonator filter/diplexer is proposed. The multiplier circuit consists of a shunt capacitor and a negative phase shift. By appropriately shunt connecting a capacitor in the vicinity of an I/O port, the I/O coupling can be effectively increased. Compared to conventional approaches of increasing I/O coupling for a wideband application, using the multiplier circuit allows much less perturbing the resonant frequency of the first resonator. For many resonator configurations such as helical resonator, to which the tapping probe could not be adjusted continuously, the multiplier circuit provides a convenient way to control I/O coupling. In this paper, the working mechanism of the proposed circuit is well proved theoretically. The usefulness of the multiplier circuit has been demonstrated for coaxial combline cavity resonators and helical resonators, both for filter and diplexer applications. As a practical example, the multiplier circuit is applied to a wideband UHF helical resonator diplexer.

**Index Terms**—Comblin resonator, diplexer, helical resonator, input/output (I/O) coupling, multiplier circuit.

## I. INTRODUCTION

THE coaxial combline resonators have been widely used to design filters/diplexers in telecommunication industry. The probes and tapped lines are two commonly used input/output (I/O) coupling structures. The tapped line I/O coupling was first described in [1] for small-percentage bandwidth (BW) interdigital filters. Nevertheless, the tapped-line I/O coupling is also suitable for moderate and wide BW applications [2]–[4] because it can provide a larger coupling than that can be achieved by coupled-line coupling for planar realization or a probe I/O coupling for the nonplanar implementation. A major problem with the tapped-line I/O coupling is that a high tapping position for realizing a large I/O coupling will drastically increase the resonant frequency of the coupled resonator, which might be tuned down by

increasing the insertion depth of frequency tuning screw or the electrical length of resonator. To realize the common input of a diplexer, the three-port junction can be of either resonant type or nonresonant type [5]. In coupled coaxial cavities, a nonresonant type of junction can be realized by a taped wire T-junction or a detuned resonator.

Helical resonator filters are commonly used in very high-frequency/UHF communication systems for their compact size and low mass as compared with waveguide cavity and coaxial resonators, and for their relatively high unloaded  $Q$  and good power handling capability as compared with the lumped element and planar transmission line resonators [6]. It has been demonstrated in [7] and [8] that helical resonators can be used in a similar manner as coaxial resonators for the narrow and moderate BW bandpass filters. A diplexer comprising two narrowband closely spaced channels in 164–175 MHz was reported in [9]. The challenges in designing a wideband helical resonator filter/diplexer lie in achieving a relative large coupling, particularly a large I/O coupling. Generally, the tapped-line I/O structure can also be applied to helical resonators to realize a large I/O coupling. However, on the one hand, the resonant frequency of the coupled resonator could be seriously perturbed. On the other hand, not every point on the resonator is conveniently accessible.

In this paper, an I/O coupling multiplier circuit for a wideband filter/diplexer is proposed and theoretically investigated for the first time. The multiplier circuit consists of a shunt capacitor and a negative phase shift. With appropriately shunt connecting a capacitor at the I/O port, a large multiplier factor for the I/O coupling can be achieved. Interestingly, the multiplier circuit perturbs very little the resonant frequency of the coupled resonator as compared with the conventional tapped-line structure. Varying the shunt capacitance, the I/O coupling can be continuously changed without adjusting the tapping positions, which is a very convenient way to adjust an I/O coupling with a great flexibility. This new concept is very useful for a wideband diplexer/filter application and is demonstrated by designing and prototyping a wideband compact but high- $Q$  helical resonator diplexer working in an UHF band.

By applying the proposed multiplier circuit, the shunt connected capacitor can be realized by a microstrip disk inside or outside the resonator cavity. However, when the shunt capacitive disk is implemented outside, the I/O coupling can be easily adjusted without accessing the internal I/O tapping wire, which facilitates the tuning of cavity filters

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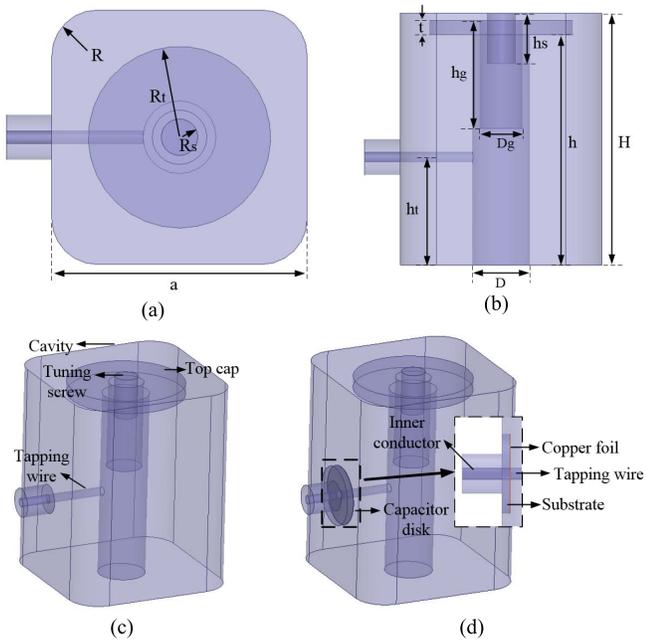


Fig. 1. Tapped I/O configuration of a combline resonator. (a) Top view. (b) Side view. (c) Perspective view. (d) I/O coupling multiplier circuit with a close-up view of the physical connection.

and diplexers by avoiding the inconvenience of opening the cavity. Although the I/O circuit with a shunt capacitor is mentioned briefly in an International Microwave Symposium (IMS) conference paper [10], in which the emphasis is placed on the structure design of a high- $Q$  wideband helical diplexer, the working mechanism of this I/O multiplier circuit and the theory behind are investigated in this paper for the first time. Besides, the applications of the proposed I/O multiplier circuit to coaxial and helical types of resonator are discussed in great detail in this paper. A good performance of the prototype of a wideband helical diplexer demonstrates that the proposed new I/O coupling multiplier circuit is a useful circuit element for realizing a wideband helical diplexer. It is anticipated that the I/O multiplier circuit can be widely used in many wideband filter/diplexer applications with a wide range of resonator configurations.

## II. I/O COUPLING MULTIPLIER CIRCUIT

Before discussing the equivalent I/O coupling value of the proposed I/O multiplier circuit, it is advisable to examine the benefits of the circuit to some commonly used I/O structures.

### A. I/O Multiplier Circuit for Filters

Consider an I/O coupling for a coupled combline resonator filter. Fig. 1(a)–(c) shows a conventional probe tapped I/O coupling structure for a combline filter, where the inner conductor of the input cable is directly tapped onto the resonator. A top-loaded coaxial resonator is used to reduce the height of the resonator. For comparison purpose, an I/O multiplier circuit is added to the same I/O port as shown in Fig. 1(d), where a shunt parallel plate capacitor is added at a location closest to the I/O port of the coupled combline resonator.

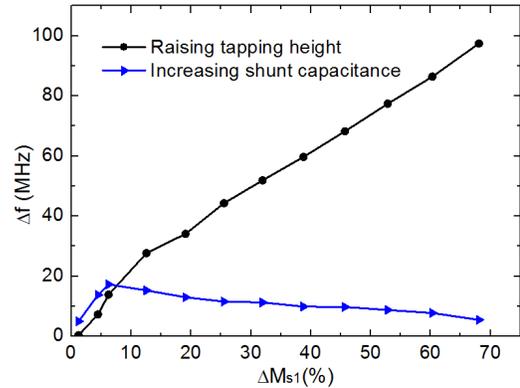


Fig. 2. Resonant frequency versus percentage increment of I/O coupling using conventional and shunt capacitor approaches for increasing I/O coupling of a tapped I/O to a combline resonator.

It is shown in Fig. 1(d) that a shunt capacitor is installed inside the cavity. The capacitor is realized by a microstrip disk whose ground is touched to the inner surface of the metal body of the filter and the disk is soldered to the inner conductor of the feeding cable. The substrate for the parallel-plate capacitor has a dielectric constant  $\epsilon_r = 3$  and thickness of 1 mm. The dimensions for the cavity are:  $a = 28$  mm,  $H = 35$  mm, and  $R = 5$  mm. The other dimensions of the resonator are as follows:  $h = 32$  mm,  $h_g = 15$  mm,  $h_s = 7$  mm,  $D = 8$  mm,  $D_g = 6$  mm,  $t = 2$  mm,  $R_s = 2$  mm, and  $R_t = 10$  mm. The initial tapping height is  $h_t = 15$  mm, and the extracted I/O coupling and resonant frequency of the tapped I/O structure are 0.6112 and 772.7 MHz referring to the center frequency  $f_0 = 814$  MHz and  $BW = 270$  MHz. There are two approaches to enlarge the I/O coupling: 1) increasing the tapping height  $h_t$ , and 2) increasing the radius of the capacitor disk. The changes of resonant frequency  $\Delta f$  versus the percentage increment of I/O coupling for the two approaches are compared in Fig. 2. The enhancement of I/O coupling value  $M_{s1}$  is represented by the percentage increment  $\Delta M_{s1}$  (%). As can be observed, the change of resonant frequency by increasing shunt capacitance is much less than that by raising the tapping height of the I/O probe.

Fig. 3(a) shows the conventional tapped I/O configuration for a helical resonator, and Fig. 3(b)–(d) shows the enhanced version of the tapped probe I/O configuration with a shunt capacitor. The helical resonator is within a rectangular cavity with length  $a = 32$  mm, width  $b = 20$  mm, height  $H = 26$  mm, and radius of round corner  $R = 5$  mm. The helical resonator has 3.3 turns, and other dimensions are as follows:  $B = 5.3$  mm,  $h_s = 10$  mm,  $h_t = 8.68$  mm,  $p = 4.5$  mm,  $L = 13$  mm,  $s = 4$  mm,  $d = 11$  mm,  $d_r = 2.5$  mm, and  $d_t = 1.2$  mm. For the conventional configuration shown in Fig. 3(a), the extracted I/O coupling and resonant frequency are 0.6941 and 736.9 MHz, respectively, referring to the center frequency  $f_0 = 814$  MHz and  $BW = 270$  MHz. By rotating the helical resonator and raising the tapping height  $h_t$ , the I/O coupling can be increased. However, the I/O coupling can be easily increased by increasing the capacitance of the shunt-connected capacitor disk shown in Fig. 3(b). The changes of

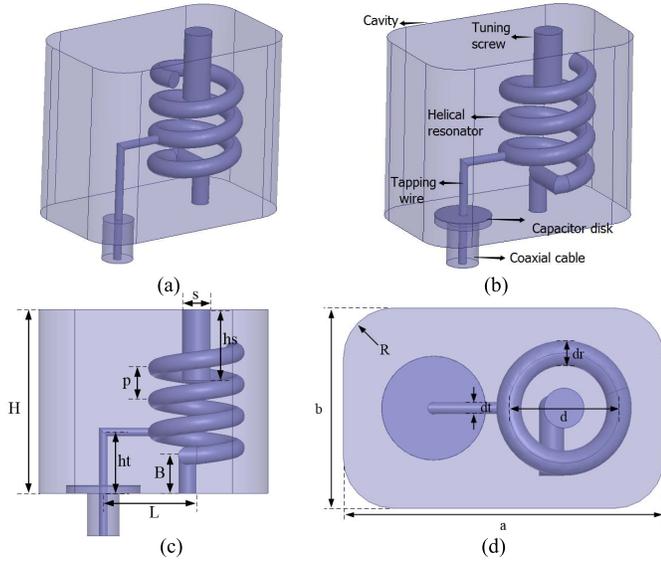


Fig. 3. Tapped I/O configuration for a helical resonator. (a) Conventional tapped I/O. (b) Tapped I/O with a coupling multiplier circuit realized by a microstrip capacitor disk. The tapped I/O of a helical resonator with I/O multiplier circuit. (c) Side view. (d) Top view with dimensional parameters.

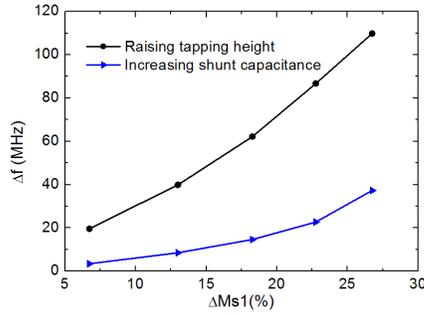


Fig. 4. Resonant frequency versus percentage increment of the I/O coupling for conventional and shunt capacitor approaches for increasing I/O coupling of tapped I/O for a helical resonator.

resonant frequency  $\Delta f$  versus the percentage increment of I/O coupling for the two I/O configurations are compared in Fig. 4. As can be observed, the change of resonant frequency is much less sensitive when a shunt capacitor is used. Moreover, the multiplier circuit is capable of continuously adjusting I/O coupling without changing the tapping position. This feature is particularly convenient for the helical resonator because not every point on the helical resonator is easily accessible without rotating the resonator.

The effect of the shunt capacitor can be analyzed using the circuit models shown in Fig. 5. In Fig. 5(a), the multiplier circuit consists of a shunt capacitor cascaded to a negative phase shifter  $\theta$  preceding the impedance inverter that realizes the I/O coupling to be magnified. Note that  $C_n$  is the normalized capacitance of the physical capacitance  $C$  with respect to the reference admittance  $Y_0$  of the port, or  $C_n = C/Y_0$ . Both I/O coupling and self-coupling of the resonator are normalized with respect to the given center frequency  $f_0$  and fractional BW (FBW). The self-coupling represents the shift of the resonator frequency from the center frequency of filter, and

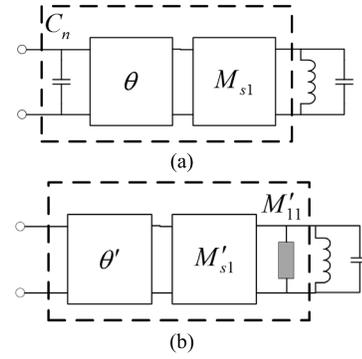


Fig. 5. (a) Circuit model of the I/O coupling multiplier circuit. (b) Equivalent I/O coupling circuit model.

can be expressed as follows:

$$M_{ii} = -\frac{1}{\text{FBW}} \left( \frac{f_r}{f_0} - \frac{f_0}{f_r} \right) \quad (1)$$

where  $f_r$  is the resonant frequency of the resonator.

An equivalent circuit shown in Fig. 5(b) can be used in a moderate frequency BW. The equivalence of the two circuits shown in Fig. 5(a) and (b) can be established by equating the  $ABCD$  matrixes of the circuits in the dashed-line boxes, which can be found to be

$$\begin{aligned} & \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \\ &= \begin{bmatrix} 1 & 0 \\ j\omega C_n & 1 \end{bmatrix} \begin{bmatrix} \cos \theta & j \sin \theta \\ j \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} 0 & j/M_{s1} \\ jM_{s1} & 0 \end{bmatrix} \\ &= \begin{bmatrix} -M_{s1} \sin \theta & j \cos \theta / M_{s1} \\ -j\omega C_n M_{s1} \sin \theta + j M_{s1} \cos \theta & -\omega C_n \cos \theta / M_{s1} - \sin \theta / M_{s1} \end{bmatrix} \end{aligned} \quad (2)$$

for the original multiplier circuit model, and

$$\begin{aligned} & \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \\ &= \begin{bmatrix} \cos \theta' & j \sin \theta' \\ j \sin \theta' & \cos \theta' \end{bmatrix} \begin{bmatrix} 0 & j/M'_{s1} \\ jM'_{s1} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jM'_{11} & 1 \end{bmatrix} \\ &= \begin{bmatrix} -M'_{s1} \sin \theta' - M'_{11} \cos \theta' / M'_{s1} & j \cos \theta' / M'_{s1} \\ jM'_{s1} \cos \theta' - jM'_{11} \sin \theta' / M'_{s1} & -\sin \theta' / M'_{s1} \end{bmatrix} \end{aligned} \quad (3)$$

for the equivalent circuit model, respectively.

The I/O coupling value and the self-coupling of the resonator in the equivalent circuit can be found as

$$M'_{s1} = \frac{M_{s1}}{\sqrt{\omega^2 C_n^2 \cos^2 \theta + 2\omega C_n \sin \theta \cos \theta + 1}} \quad (4)$$

$$M'_{11} = M_{s1}^2 \left( \tan \theta - \frac{\omega C_n + \tan \theta}{\omega^2 C_n^2 \cos^2 \theta + 2\omega C_n \sin \theta \cos \theta + 1} \right) \quad (5)$$

with

$$\tan \theta' = \tan \theta + \omega C_n. \quad (6)$$

Notice that the parameters in the equivalent circuit are frequency-dependent. Considering (6) and comparing terms

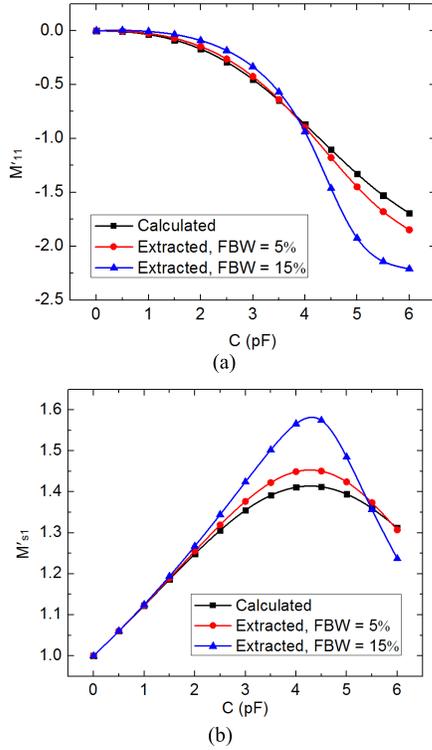


Fig. 6. Equivalent (a) self-coupling and (b) I/O coupling versus shunt capacitance obtained by analytical calculation and curve-fitting extraction.

“B” in (2) and (3), it can be seen that I/O coupling increases if

$$|\tan \theta| > |\omega C_n + \tan \theta| \quad (7)$$

which means that for a fixed  $\theta$ , the maximum multiplier factor can be found to be

$$\max \left( \frac{M'_{s1}}{M_{s1}} \right) = \left| \frac{1}{\cos \theta} \right|, \quad \text{when } C_n = \frac{-\tan \theta}{\omega}. \quad (8)$$

It is worthwhile to elaborate inequality (7), which is held only when  $\tan \theta < 0$ . For  $|\theta| < \pi/2$ ,  $\tan \theta < 0$  means  $\theta < 0$ . In fact, the phase shift  $\theta$  is contributed by two things: the phase loading at the port, which is caused by the higher order modes at the discontinuity [11], and a short-section transmission line. According to our experience in computer-aided tuning of coupled-resonator filters and diplexers, the phase loadings for most practical filters and diplexers are negative values. Therefore, as long as the phase contributed by the short section of transmission line is smaller than the phase loading, inequality (7) can be held. It is understandable that if the phase loading is uncontrollable, so is  $\theta$ .

For illustration purpose, consider the cases in which the resonant frequency  $f_0 = 0.744$  GHz,  $\text{FBW} = 5\%$  and  $15\%$ , and  $\theta = -\pi/4$ . The equivalent coupling can be either calculated using (4)–(6) at a specific frequency, say  $f_0$ , or extracted by fitting the responses of the two circuits in the frequency band of interest. Since (4)–(6) does not depend on FBW, as shown in Fig. 6, the couplings obtained by the two methods agree well with each other for a small FBW. Some discrepancies can be observed when FBW becomes large. This is because the equivalent parameters in (4)–(6) are

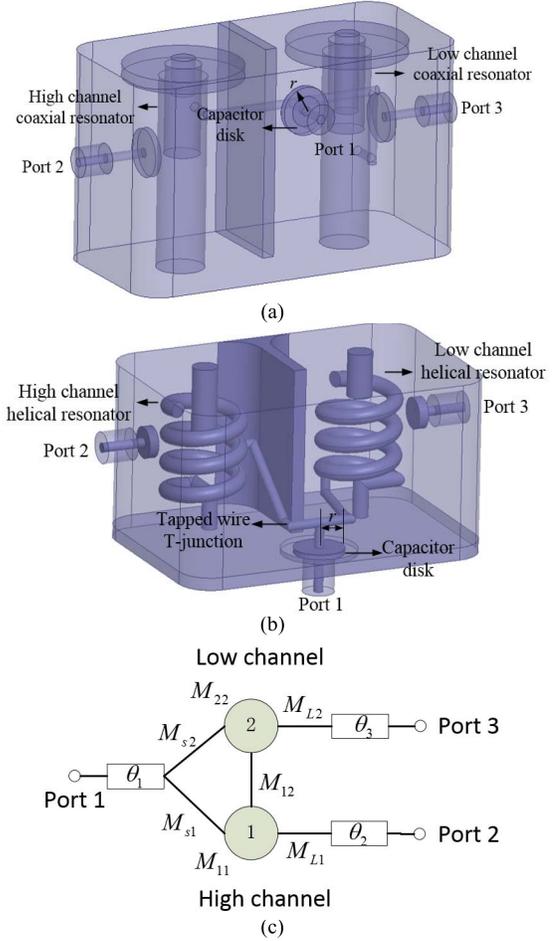


Fig. 7. Practical I/O coupling multiplier circuit at the common port of (a) combine coaxial resonator diplexer, (b) helical resonator diplexer, and (c) equivalent circuit model.

frequency-dependent and are calculated at  $f_0$ , while they are assumed to be constant in the curve-fitting extraction. It is shown in Fig. 6(a) that the change of self-coupling  $M'_{s1}$  is not significant in the range of  $C < 3$  pF, in which  $M'_{s1}$  linearly increases with  $C$ . Fig. 6(b) shows a clear trend that the equivalent I/O coupling increases as  $C$  increases with a predictable maximum.

### B. I/O Multiplier Circuit at Common Port of Diplexer

A tapped wire  $T$ -junction configuration is widely used at the common port of a diplexer. Fig. 7 shows two practical common port tapped  $T$ -junctions, with the I/O coupling multiplier circuit, for both combine coaxial resonator and helical resonator diplexers and their equivalent circuit model.  $\theta_1$ ,  $\theta_2$ , and  $\theta_3$  represent the equivalent phase shift at the three ports. To reflect the parasitic coupling between the two resonators that are coupled to the common port by the  $T$ -junction, mutual coupling  $M_{12}$  between the two resonators is introduced.

The I/O coupling multiplier circuit applied at the common port is implemented by a microstrip disk capacitor. To extract the equivalent coupling value from electromagnetic (EM) simulation for different radius  $r$  of the capacitor disk (with substrate of  $\epsilon_r = 3$  and thickness  $h = 0.76$  mm), a weakly coupled port is added to each of the resonators in the EM

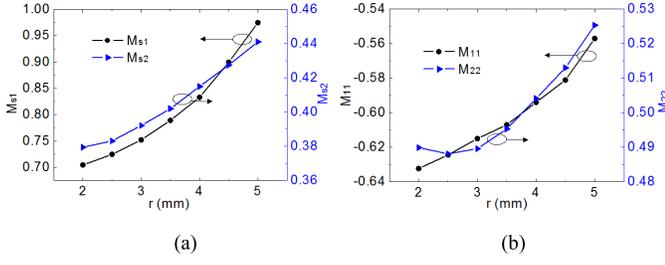


Fig. 8. Extracted (a) I/O couplings and (b) self-couplings versus  $r$  for the combline resonator diplexer.

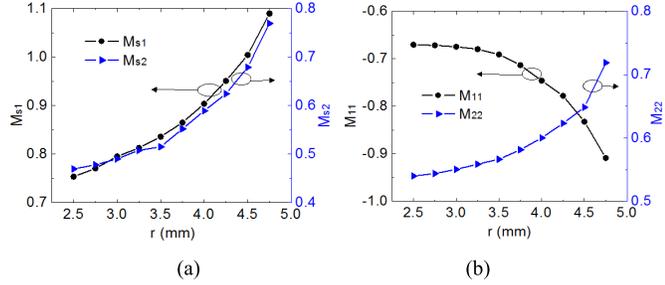


Fig. 9. Extracted (a) I/O couplings and (b) self-couplings versus  $r$  for the helical resonator diplexer.

model denoted as ports 2 and 3, respectively. The parameter extraction is done by curve-fitting the three-port S-parameters of the physical model and those of the circuit model. The extracted normalized I/O couplings and the self-couplings versus  $r$  (mm) for the combline resonator diplexer and the helical resonator diplexer are plotted in Figs. 8 and 9, respectively. Here, the normalized couplings are referred to  $f_0 = 0.814$  GHz and  $BW = 0.27$  GHz. It can be observed that as  $r$  increases, both I/O couplings  $M_{s1}$  and  $M_{s2}$  increase. In the case of combline resonator diplexer, the resonant frequencies of the high and low channel resonators change only at 11 and 4.6 MHz, respectively, when  $M_{s1}$  increases by 38% and  $M_{s2}$  increases by 16%. In the case of helical resonator diplexer, the resonant frequencies of the high and low channel resonators change at 36 and 22 MHz, respectively, when  $M_{s1}$  increases by 44%, and  $M_{s2}$  increases by 64%.

The equivalence of the multiplier circuit at the common port can be analyzed by matching the I/O circuit with the multiplier circuit shown in Fig. 10(a) to its equivalent circuit shown in Fig. 10(b). Following the definition, it is straightforward to find the admittance matrix of original circuit model as

$$[Y] = \begin{bmatrix} j\omega C_n + j \tan \theta & jM_{s1} \sec \theta & jM_{s2} \sec \theta \\ jM_{s1} \sec \theta & jM_{s1}^2 \tan \theta & jM_{s1} M_{s2} \tan \theta + jM_{12} \\ jM_{s2} \sec \theta & jM_{s1} M_{s2} \tan \theta + jM_{12} & jM_{s2}^2 \tan \theta \end{bmatrix} \quad (9)$$

whereas the admittance matrix of the equivalent circuit is

$$[Y'] = \begin{bmatrix} j \tan \theta' & jM'_{s1} \sec \theta' & jM'_{s2} \sec \theta' \\ jM'_{s1} \sec \theta' & jM'^2_{s1} \tan \theta' + j \Delta B_1 & jM'_{s1} M'_{s2} \tan \theta' + jM'_{12} \\ jM'_{s2} \sec \theta' & jM'_{s1} M'_{s2} \tan \theta' + jM'_{12} & jM'^2_{s2} \tan \theta' + j \Delta B_2 \end{bmatrix} \quad (10)$$

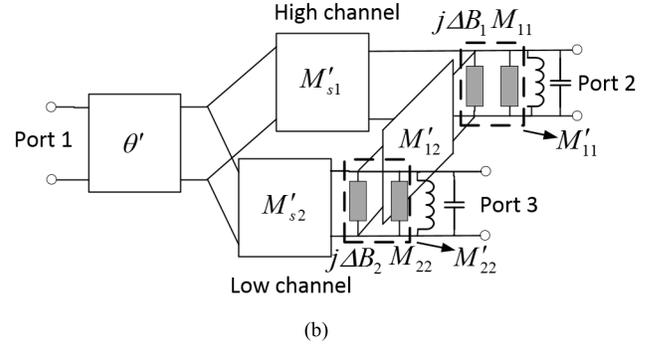
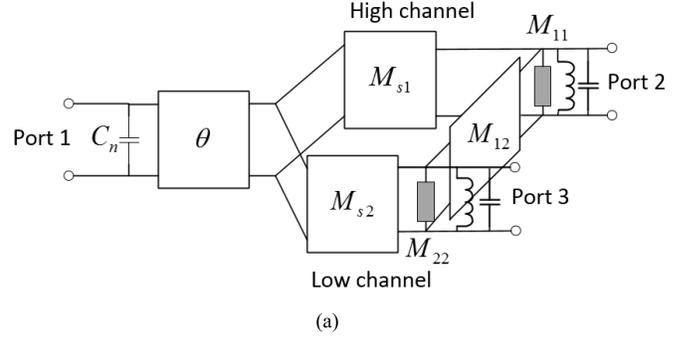


Fig. 10. Circuit model of the multiplier circuit at common port  $T$ -junction. (a) Original I/O coupling multiplier circuit. (b) Equivalent circuit of (a).

Equating (9) and (10) leads to

$$\tan \theta' = \omega C_n + \tan \theta \quad (11)$$

$$M'_{s1} = \frac{M_{s1}}{\sqrt{\omega^2 C_n^2 \cos^2 \theta + 2\omega C_n \sin \theta \cos \theta + 1}} \quad (12)$$

$$M'_{s2} = \frac{M_{s2}}{\sqrt{\omega^2 C_n^2 \cos^2 \theta + 2\omega C_n \sin \theta \cos \theta + 1}} \quad (13)$$

$$M'_{12} = \frac{1}{2} M_{s1} M_{s2} \frac{\omega^2 C_n^2 \sin 2\theta - 2\omega C_n \cos 2\theta}{\omega^2 C_n^2 \cos^2 \theta + 2\omega C_n \sin \theta \cos \theta + 1} + M_{12} \quad (14)$$

$$\Delta B_1 = M_{s1}^2 \left( \tan \theta - \frac{\omega C_n + \tan \theta}{(\omega C_n \cos \theta)^2 + \omega C_n \sin 2\theta + 1} \right) \quad (15)$$

$$\Delta B_2 = M_{s2}^2 \left( \tan \theta - \frac{\omega C_n + \tan \theta}{(\omega C_n \cos \theta)^2 + \omega C_n \sin 2\theta + 1} \right). \quad (16)$$

As can be seen from (11)–(16), the I/O couplings and self-couplings follow the same relationship with  $C_n$  as those in (4)–(6). Obviously, the equivalent mutual coupling  $M'_{12}$  will also vary with  $C_n$ .

### III. EXAMPLE OF A WIDEBAND HELICAL DIPLEXER

#### A. Circuit Model Design

This example involves the design of a wideband helical diplexer with a 36% FBW. This diplexer is used to combine LTE and GSM services. The lower frequency band is 690–803 MHz, whereas the upper frequency band is 824–960 MHz. The required return loss in each band is less than 20 dB, and isolation between two bands is larger than 30 dB. The insertion loss should be less than 0.4 dB in 690–793 and 834–960 MHz, and less than 0.6 dB in 793–803 and 824–834 MHz. To realize such a wideband diplexer,

TABLE I  
 OPTIMIZED TARGET COUPLING MATRIX

	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	1	2	3	4	5	6	7	8	9	10
P <sub>1</sub>	0	0	0	0	0	0	0	0.5619	0.9091	0	0	0	0
P <sub>2</sub>	0	0	0	0.7357	0	0	0	0	0	0	0	0	0
P <sub>3</sub>	0	0	0	0	0	0	0	0	0	0	0	0	0.7158
1	0	0.7357	0	0.577	-0.439	0	0	0	0	0	0	0	0
2	0	0	0	-0.439	0.5775	-0.2477	0.1995	0	0	0	0	0	0
3	0	0	0	0	-0.2477	0.2199	-0.2351	0	0	0	0	0	0
4	0	0	0	0	0.1995	-0.2351	0.6113	-0.3695	0	0	0	0	0
5	0.5619	0	0	0	0	0	-0.3695	0.8446	0.2788	0	0	0	0
6	0.9091	0	0	0	0	0	0	0.2788	-0.677	-0.4438	0	0	0
7	0	0	0	0	0	0	0	0	-0.4438	-0.618	-0.2424	-0.196	0
8	0	0	0	0	0	0	0	0	0	-0.2424	-0.229	-0.2496	0
9	0	0	0	0	0	0	0	0	0	-0.196	-0.2496	-0.583	-0.4246
10	0	0	0.7158	0	0	0	0	0	0	0	0	-0.4246	-0.587

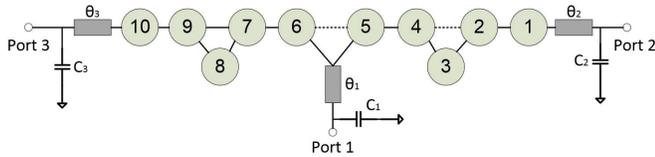


Fig. 11. Coupling diagram of the wideband helical diplexer. Solid line: capacitive coupling. Dotted line: inductive couplings.

large value coupling elements must be realized in a compact way. Therefore, the multiplier circuits are added at each port. Considering the very narrow guard band, a transmission zero is introduced in each channel filter by using a trisection coupling block as shown in Fig. 11.

Since a tapped  $T$ -junction I/O coupling is adopted, the parasitic inductive mutual coupling  $M_{56}$  between resonators 5 and 6 at the common port is inevitable and is incorporated in the circuit design. As discussed in [12], the circuit model of a  $T$ -junction can be either a non-resonant-node junction or a  $\Delta$ -model where the two first resonators are coupled to each other. With a reasonable value of  $M_{56}$  in Fig. 11, a satisfactory diplexer performance can be obtained by optimizing other coupling elements. Extracted from an EM simulation response of an initial design of the I/O structure at the common port, the initial target coupling matrix is optimized with  $M_{56}$  fixed as 0.2788.

Table I gives the optimized coupling matrix, where the center frequency is  $f_0 = 0.8139$  GHz and  $FBW = 0.3317$ . The unloaded  $Q$  for each resonator is set as 800. Fig. 12 shows the responses corresponding to the optimized coupling matrix. It is worth mentioning that the optimized coupling matrix is just for the initial EM model design of diplexer, and does not include the stray couplings that usually exist in fabricated prototype as highlighted in red in Table II.

### B. Physical Design of the Diplexer

The design details of the wideband helical diplexer have been reported in a recent IMS paper [10]. To provide a complete design outline in this paper, only the key considerations are highlighted here.

A set of empirical design formulas for helical resonators are available in [6]. All the capacitive couplings are realized by placing two helical resonators wound in the same direction close to each other. A tuning screw can be placed between the two resonators for fine tuning of the mutual coupling. It can

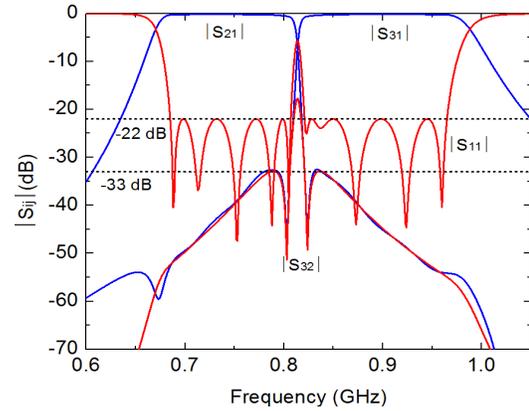


Fig. 12. Responses of the initially designed target coupling matrix.

be found that when the two helical resonators are wound in opposite directions, the coupling value is much smaller as compared to that of the same direction case. It can also be found that the capacitive coupling depends on the starting winding angles of the two coupled helical resonators. The inductive coupling is realized by a coupling wire tapped to the bottom of the two coupled helical resonators. Such coupling configuration provides both inductive and capacitive couplings but is dominated by inductive coupling. The coupling strength of the inductive coupling can be controlled by changing the tapping position of coupling wire. Generally, the higher the tapping position is, the stronger the inductive coupling will be. For fine tuning of the total coupling, the tuning screw placed between the coupled resonators can be exploited to provide a certain amount of adjustment.

The I/O coupling multiplier circuits at each filter port and the common port are implemented using the configurations suggested in Figs. 3 and 7, respectively. The capacitor is realized by a microstrip capacitor disk that is soldered to the inner conductor of the interfacing cables. The ground plane of the disk is touched to the metal body of the diplexer. The disk can be installed inside or outside the resonator cavity. However, the outside option provides a great convenience for continuous tuning of an I/O coupling without opening the cavity. Fig. 13 shows the detailed structure of the diplexer, of which each helical resonator has the same dimensions as that of the helix in Fig. 3, but different turn arrangements for each resonator, as listed in Table III, are used. The numbering of resonators is in accordance with that in the schematic shown in Fig. 11. The overall dimensions of diplexer and

TABLE II  
EXTRACTED COUPLING MATRIX CORRESPONDING TO THE FABRICATED PROTOTYPE

	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	1	2	3	4	5	6	7	8	9	10
P <sub>1</sub>	0.0702	0	0	0	0	0	0.045	0.5503	1.0383	-0.126	-0.0015	0	0
P <sub>2</sub>	0	0.0051	0	0.7345	0	0	0	0	0	0	0	0	0
P <sub>3</sub>	0	0	0.0019	0	0	0	0	0	0	0	0	0	0.7322
1	0	0.7345	0	0.5756	-0.4448	0	0	0	0	0	0	0	0
2	0	0	0	-0.4448	0.5849	-0.2566	0.2118	0	0	0	0	0	0
3	0	0	0	0	-0.2566	0.1975	-0.2416	0	0	0	0	0	0
4	0.045	0	0	0	0.2118	-0.2416	0.6395	-0.418	-0.0122	-0.002	0	0	0
5	0.5503	0	0	0	0	0	-0.418	0.9199	0.4183	0	0	0	0
6	1.0383	0	0	0	0	0	-0.0122	0.4183	-0.429	-0.4935	0	0	0
7	-0.126	0	0	0	0	0	-0.002	0	-0.4935	-0.696	-0.2503	-0.207	0
8	-0.0015	0	0	0	0	0	0	0	-0.2503	-0.219	-0.2641	0	0
9	0	0	0	0	0	0	0	0	0	-0.207	-0.2641	-0.555	-0.4512
10	0	0	0.7322	0	0	0	0	0	0	0	0	-0.4512	-0.547

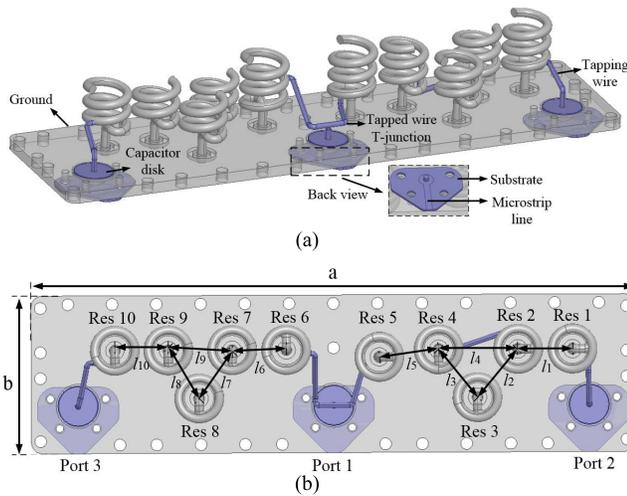


Fig. 13. Structure details of the diplexer (with cavity cover removed). (a) Perspective view. (b) Top view.

spacing among adjacent resonators are shown in Table IV. It is worth mentioning that the three capacitor disks installed at common port and low/high channel ports are initially large enough with a margin for further tuning. The adjustment of the capacitor disk can be done by scraping off the copper foil, which equivalently reduces the shunt capacitance. The manual tuning of prototype diplexers is done with the help of the in-house computer-aided tuning software. A fabricated prototype diplexer after tuning is shown in Fig. 14 with details of the capacitor disks. As can be observed, the capacitor disk at port 1 has been cut out by about a quarter. The capacitor disk at port 3 remains intact, whereas the capacitor disk at port 2 is almost removed. It is worth mentioning that the areas of installed capacitor disks to achieve the required I/O couplings are estimated with  $M_{56} = 0.2788$  extracted from the EM model. Therefore, it is understandable that significant tuning may be needed for some capacitor disks, for instance, the capacitor disk at port 2 here, as the extracted  $M_{56}$  in the final tuning stage differs from that value.

### C. I/O Multiplier Circuits and Measurement Results

From the EM model, without the multiplier circuits, the extracted phase  $\theta$  is around  $-42^\circ$  at the common port, and around  $-20^\circ$  at two channel filter ports. According to

TABLE III  
TURNS OF EACH HELICAL RESONATOR

Resonator	1	2	3	4	5
Turns	3.3	3	2.8	3	3.3
Resonator	6	7	8	9	10
Turns	3.3	2.3	2.3	2.3	2.8

TABLE IV  
DIMENSIONAL PARAMETERS OF DIPLEXER (IN MILLIMETERS)

$a = 164$	$b = 42.6$	$l_1 = 14.8$	$l_2 = 17.03$	$l_3 = 16.71$	$l_4 = 21.5$
$l_5 = 16.22$	$l_6 = 14.7$	$l_7 = 15.81$	$l_8 = 15.42$	$l_9 = 17.3$	$l_{10} = 14.5$

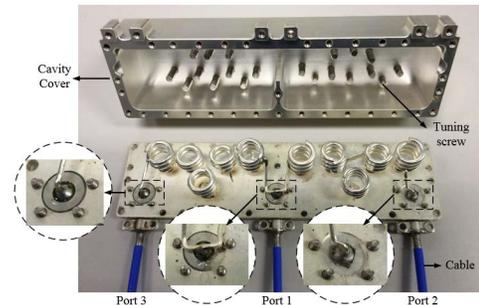


Fig. 14. Photograph of the fabricated prototype of the wideband helical resonator diplexer.

(8), the maximum multiplier factors are 1.345 for the I/O couplings at the common port, and 1.064 at two channel filter ports. Therefore, with I/O multiplier circuits, the I/O coupling at the common port can be greatly enhanced, whereas the I/O couplings at two channel filter ports are marginally affected. The measured response of the prototype diplexer is shown in Fig. 15, and its corresponding coupling matrix is extracted using the theory proposed in [13] and is given in Table II. Note that some unwanted stray couplings exist in the extracted circuit model, for instance,  $M_{17} = -0.126$ . These couplings, as shown in red in Table II, have been taken into account in reoptimizing the target coupling matrix. For comparison purpose, the response of the optimized target coupling matrix with the fixed stray couplings in Table II is superimposed in Fig. 15. A small amount of discrepancy

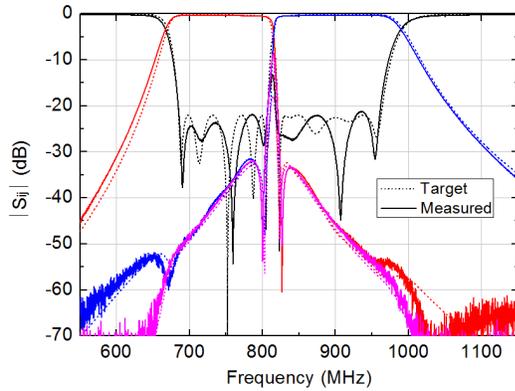


Fig. 15. Response of optimized target coupling matrix and the measured response of the prototype wideband helical resonator diplexer.

TABLE V  
COMPARISON WITH OTHER WIDEBAND DIPLEXERS

Ref.	Center freq. $f_{01}/f_{02}$ (GHz)	$FBW_1/FBW_2$ (%)	Filter order	Common junction design	Resonator type
[16]	5.25/5.95	9.52/8.40	6/6	Common transformer	Coaxial compline
[17]	0.257/0.337	17.5/13.4	6/6	Coaxial line impedance transformers	Quasi lumped
This work	0.744/0.889	15.2/15.3	5/5	Tapped-line with multiplier circuit	Helical

$f_{01}/f_{02}$ : low/high channel center frequency;  
 $FBW_1/FBW_2$ : low/high channel fractional bandwidth.

between the target response and the measurement is attributed to the discrepancy caused by the inevitable dispersion effect in a wide frequency range that could not be reflected in the coupling matrix. Nevertheless, the target coupling matrix can effectively guide the tuning to meet the specifications. The measured insertion losses are 0.34 and 0.59 dB at 690 and 803 MHz, respectively, for the low channel band. For the high channel band, the measured insertion losses are 0.59 and 0.35 dB at 824 and 960 MHz, respectively. Note that all measurements include 0.1-dB insertion loss of the connecting cables. The average unloaded  $Q$  of the helical resonators is extracted to be about 800.

#### D. Comparison Study

For a moderate or wide BW filter/diplexer, an insufficient I/O coupling usually results in a poor input match at the ports. In the literature of wideband diplexer design [14]–[17], the input match at the common port over a wide frequency range is mostly a tricky problem, especially when the diplexer is contiguous or the guard band is narrow as in the case of the example diplexer in this paper. In [14], a diplexer is constructed by a pair of high-pass/low-pass filters, which are complementary to each other, so a good match at the common port can be achieved over a broad frequency BW. In [15], it is shown that a common junction multiplexer composed of multiple-component combline filters covering multioctave frequency ranges can be built by adding extra

circuits in front of component filters to make them minimum-susceptance. However, the additional circuits make the structure complicated and the manufacturing difficult. A low-cost approach is demonstrated in [16] using a common transformer at the common port of a combline-filter diplexer. In [17], two coaxial-line impedance transformers longer than  $1/6$  of wavelength are inserted between each channel filter and the junction at the common port in order to achieve a wideband matching. Compared to the approaches in [16] and [17] (Table V), the proposed tapped-line I/O coupling structure in conjunction with the I/O multiplier circuit offers a more convenient and compact solution to the wideband I/O coupling for wideband filters or diplexer.

#### IV. CONCLUSION

In this paper, a novel I/O coupling multiplier circuit is proposed, and its working mechanism and design formula have been thoroughly investigated theoretically and experimentally. The superiority of the multiplier circuit for increasing an I/O coupling over conventional approach of raising the tapping point has been demonstrated through the EM models. It has been shown that the I/O coupling multiplier circuit can be used at both the channel filter port and the common port of a diplexer. If the shunt capacitor is installed outside the cavity, the multiplier circuit provides a new method of tuning I/O couplings without opening the cavity. The effectiveness and usefulness of the multiplier circuit have been demonstrated through a design example of wideband UHF helical resonator diplexer and EM simulation of coaxial combline filters. It should be pointed out that the proposed multiplier circuit is mainly applicable to the I/O coupling with a large negative  $\theta$  for  $|\theta| < \pi/2$ ; meanwhile, the maximum multiplier factor cannot be analytically predicted with high accuracy for filters and diplexers with a moderate or large FBW.

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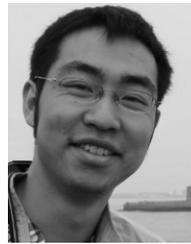
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