Department of Electronic Engineering, CUHK
Prof. Alex Leung & Prof. CS Choy
Poon Chun Fai

An Output-capacitor-less LDO With Digital Assisted Dynamic Biasing And Slew-rate Enhancement

Introduction

To reduce the chip area, output-capacitor-less design was then developed [1]-[2] which applied RC coupling to detect voltage spikes. To further decrease the chip area, utilizing two comparators to detect the voltage spikes at the output node of LDO will be presented in this poster.

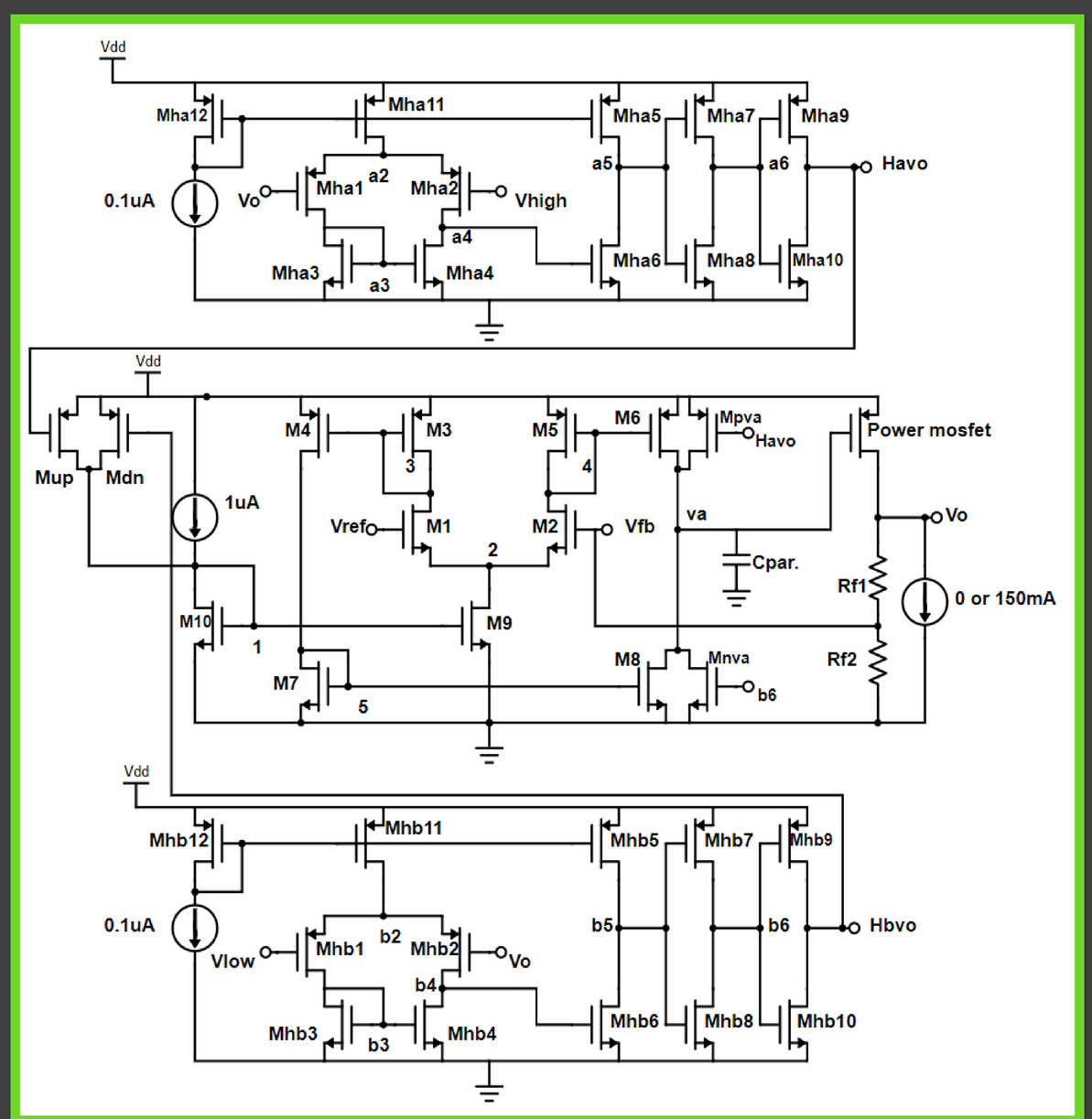

Fig. 2. Proposed circuit diagram

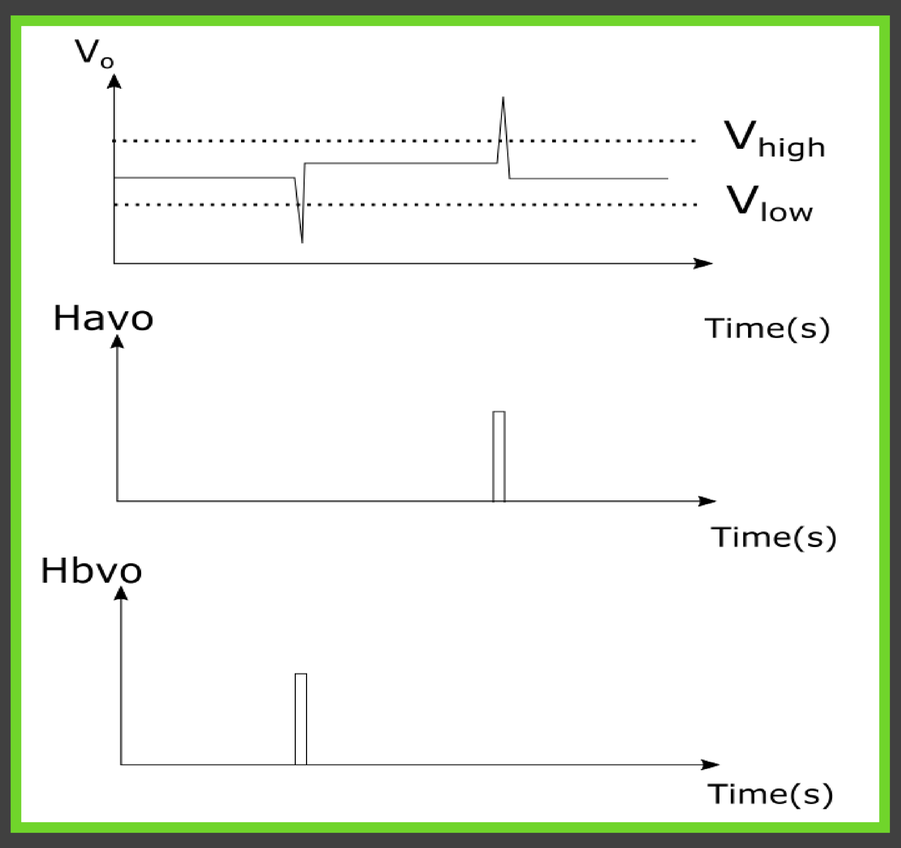

Fig. 1. Voltage spike detection by two comparators

Result

	Proposed	Conventional
Technology	0.13-μm	
Quiescent Current	12.8 μA (steady state)	12.3 μA
Gain	42.5 dB	44.16 dB
UGF	11.11 MHz	0.78 MHz
PM	81.7°	87.2°
Settling time (undershoot)	0.121μs	1.74μs
Settling time (overshoot)	0.898us	5.19 μs

Proposed approach

1 Voltage Spike Detection

Using two hysteretic comparators to detect the occurrence of undershoot and overshoot. As shown in Fig. 1. When the output voltage is lower (higher) than the threshold V_{low} (V_{high}), it would trigger one of the comparators to generate a rail to rail impulse (Havo or Hbvo) which is a commander to enable the dynamic biasing and slew-rate enhancement circuit at transient instants.

2 Dynamic Biasing

The dynamic biasing is very simple that is constructed by two p-mosfets (M_{dn} & M_{up}). Both M_{dn} and M_{up} acts as the switches. At transient instant, either M_{dn} or M_{up} will turn on by the impulse from comparators and deliver certain amount of current to the LDO. The increased current could enlarge the UGF and then reduce the response time of LDO.

3 Slew-rate Enhancement

The Slew-rate Enhancement circuit (M_{pva} & M_{nva}) will only turn on at transient instants. They are responsible to charge or discharge the most bulky parasitic capacitor (C_{par}) to rapidly adjust the V_{SG} of the power mosfet. It aims to further reduce the response time of the power mosfet during harsh loading current demand.

Conclusion

Comparing with output-capacitor-less conventional LDO, these techniques effectively reduce the settling times of undershoot and overshoot at transient instants by 93% and 82.6% respectively. The quiescent current only consume 12.8μA at steady stage.

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References

[1]M. Ho and K. N. Leung, "Dynamic bias-current boosting technique for ultralow-power low-dropout regulator in biomedical applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 3, pp. 174–178, Mar. 2011.

[2]P. Y. Or and K. N. Leung, "An output-capacitorless low-dropout regulator with direct voltage-spike detection," Solid-State Circuits, IEEE Journal of, vol. 45, no. 2, pp. 458–466, 2010.