A Multiple Cascade Cross-coupled Amplifier

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Objectives

- To enhance the speed of traditional amplifiers
- To improve the accuracy of classical amplifiers

Prior Arts

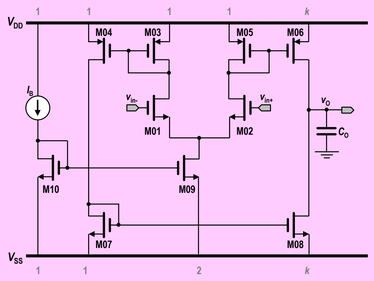


Fig. 1 Single-stage amplifier.

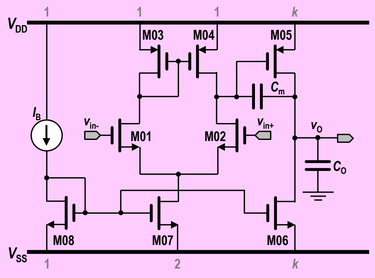


Fig. 2 Simple Miller amplifier.

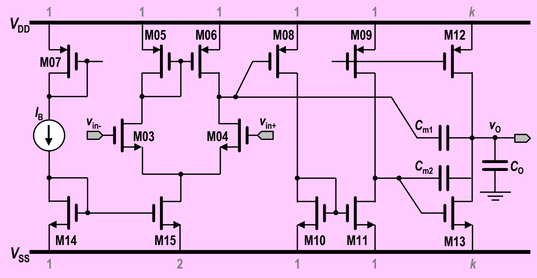
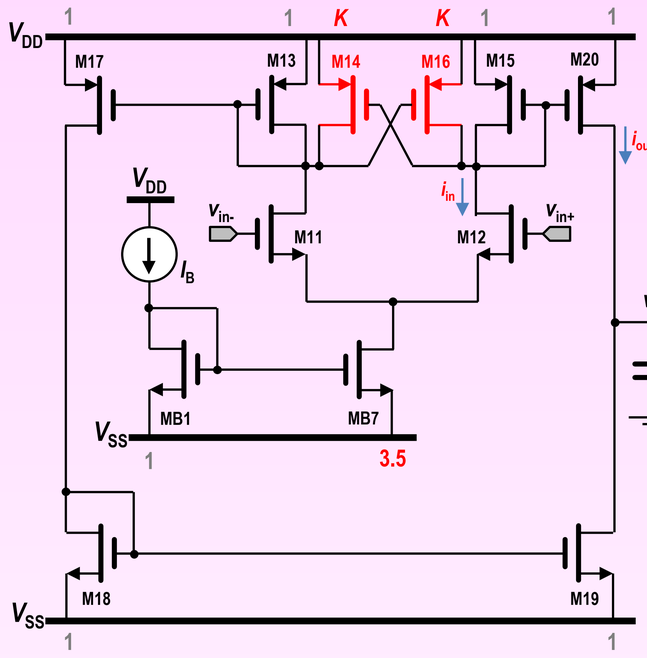


Fig. 3 Nested Miller amplifier.

	Single-Stage	SMC	NMC
Gain	$G_m R_o$	$G_{m1}G_{m2}R_{o1}R_{o2}$	$G_{m1}G_{m2}G_{m3}R_{o1}R_{o2}R_{o3}$
UGF	$\frac{G_m}{C_L}$	$\frac{G_{m2}}{2C_L}$	$\mathrm{UGF}=\frac{G_{m3}}{4C_L}$
Assumption	$C_1 << C_L$ $G_{m1}R_{o1} >> 1$	$C_1 < C_m, C_1 << C_L$ $C_m < C_L$ $G_{m1}R_{o1} >> 1$	$(C_1, C_2) < (C_{m1}, C_{m2}) < C_L$ $G_{m1}R_{o1} >> 1$ $G_{m2}R_{o2} >> 1$ $G_{m3}R_{o3} >> 1$
Compensation capacitor	N.A.	$C_m = \left(\frac{2G_{m1}}{G_{m2}}\right)\cdot C_L$	$C_{m1} = 4\left(\frac{G_{m1}}{G_{m3}}\right)\cdot C_L$ $C_{m2} = 2\left(\frac{G_{m2}}{G_{m3}}\right)\cdot C_L$

Table I. Summary of studied single-stage and frequency compensated amplifier.

Cross-coupled Cell



$$\frac{v_{gs}}{r_{o12}//r_{o15}//r_{o16}} + (g_{m15} - g_{m16})v_{gs} - i_{in} = 0$$

$$\frac{v_{gs}}{r_{o12}//r_{o15}//r_{o16}} + (g_{m15} - Kg_{m15})v_{gs} - i_{in} = 0$$

$$v_{gs}\left[\frac{1}{(1-K)g_{m15}(r_{o12}//r_{o15}//r_{o16})}+1\right] = \left[\frac{1}{(1-K)g_{m15}}\right]i_{in}$$

$$\frac{v_{gs}}{i_{in}} \approx \frac{1}{(1-K)g_{m15}}$$

$$i_{out} = g_{m20}v_{gs} = \left[\frac{g_{m20}}{(1-K)g_{m15}}\right]i_{in} = \frac{i_{in}}{(1-K)}$$

Fig. 4 Modified current mirror amplifier with cross-coupled cell.

Proposed Design — Overall Layout

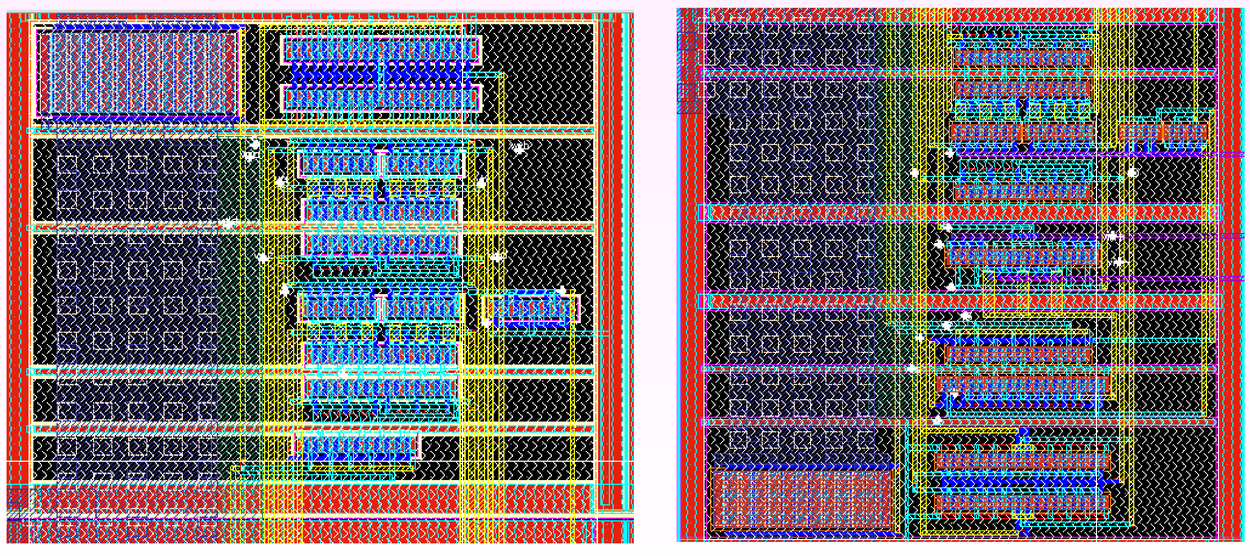


Fig. 5 Layout of the proposed multiple cascade cross-coupled amplifier.

Proposed Design

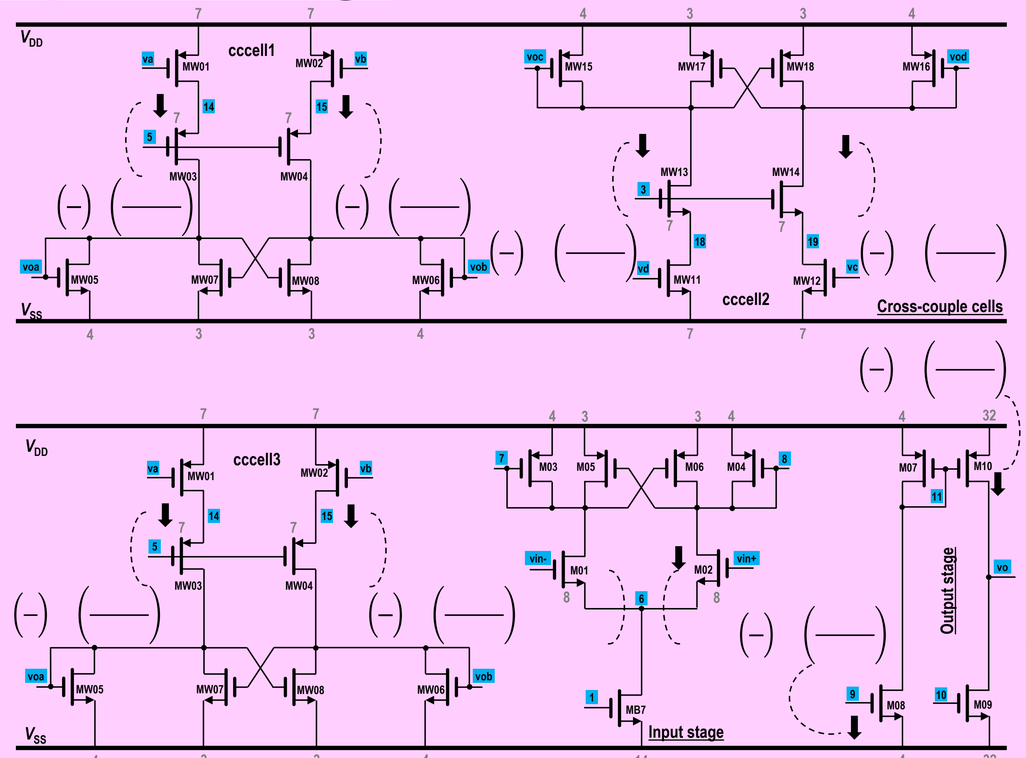


Fig. 6 Proposed multiple cascade cross-coupled amplifier with small signal flow.

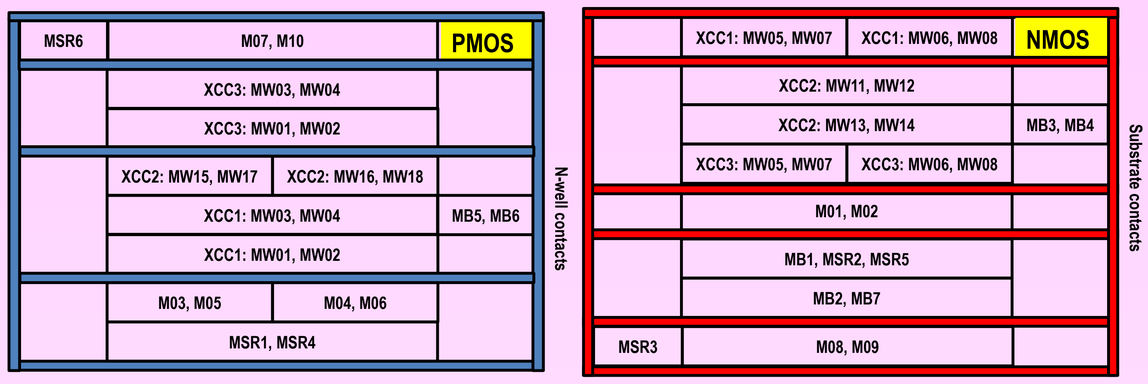


Fig. 7 Floor plan of P-type and N-type MOSFET in the proposed circuit.

Proposed Design — Simulation Results

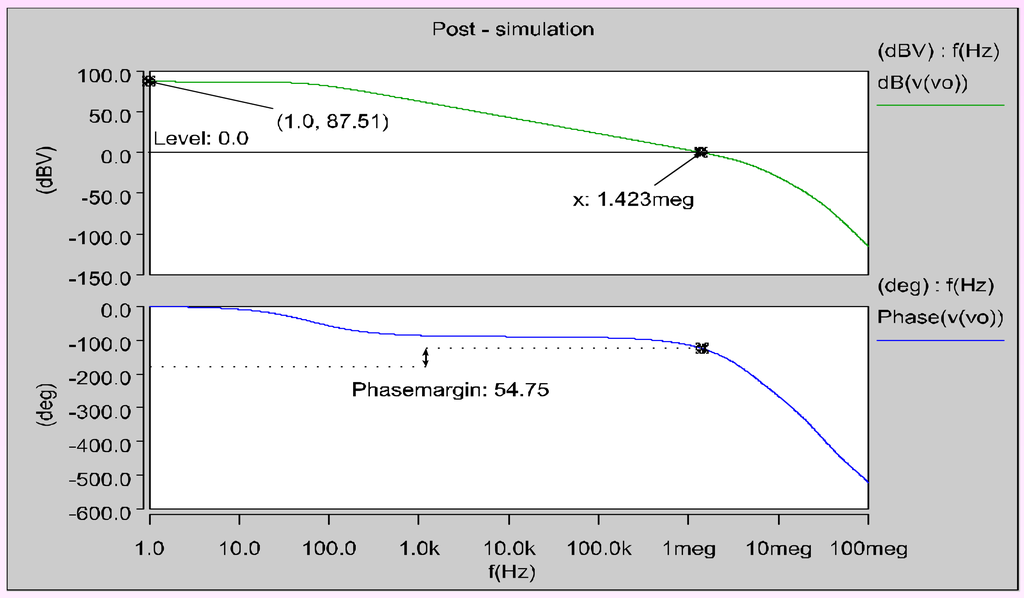


Fig. 8 Frequency response of the proposed circuit.

	CBMC JSSC'13 [5]	NCM JSSC'15 [7]	H-OTA JSSC'15 [8]			This work Pre-layout	This work Post-layout
CMOS technology (μm)	0.35	0.18	0.13			0.13	
Chip area (mm²)	0.016	0.0013	0.0027			0.0023 (35.1μm × 68.3μm)	
C_O (pF)	15000	500	10000	15000	30000	15000	
V_{DD} (V)	2	1.2	0.7			0.8	
I_{DD} (μA)	72	3	24			14.8	14.8
dc gain (dB)	>100	84	~100			86.6	86.6
GBW (MHz)	0.95	0.396	1.99	1.46	0.77	1.46	1.42
PM (°)	52.3	81.4	47	66.9	84.3	69	54.8
SR (V/μs)	0.22	0.0115	0.7	0.47	0.24	0.25	0.25
On-chip capacitance (pF)	2.6	0	0			0	
FOM_S (MHz·pF/mW)	98,958	55,000	1,184,524	1,303,571	1,375,000	1,849,662	1,806,317
FOM_L (V/μs·pF/mW)	22,917	1,597	416,667	419,643	428,571	325,846	312,186
$IFOM_S$ (MHz·pF/mA)	197,916	66,000	829,166	912,500	962,500	1,479,729	1,445,053
$IFOM_L$ (V/μs·pF/mA)	45,834	1,916	291,667	293,750	300,000	260,676	249,748

Table II. Performance summary of the proposed amplifier and reported designs.

Reference

J. Roh, S. Byun, Y. Choi, H. Roh, Y.-G. Kim, and J.-K. Kwon, "A 0.9-V 60- W 1-bit fourth-order delta-sigma modulator with 83 dB dynamic range," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 361–370, Feb. 2008.

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Conclusion

- A multiple cascade cross-couple amplifier is proposed.
- The layout of the proposed circuit has been done.
- Pre- and post- layout simulations have been conducted. The results verified the proposed ideas and circuit.
- The performance of the proposed circuit could be enhanced by changing bias transistors to signal transistors.