Department of Electronic Engineering  
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SEMINAR  
Nanoscale Electronic Synapses for Brain-Inspired Computing  
By  
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Time : 2:30pm  
Place : Room 1009, William MW Mong Engineering Building (ERB1009), CUHK

Abstract:  
Unlike classical enterprise computing that operates on structured, digital data, 21st century information technology (IT) must process, understand, classify, and organize the vast amount of data in real-time. 21st century applications will be dominated by machine-learning kernels operating on Tbytes of active data with little data locality. At the same time, massively redundant sensor arrays sampling the world around us will give humans the perception of additional “senses” blurring the boundary between biological, physical, and cyber worlds. Real-time big-data analytics, and the processing of perceptual data in wearable devices, clearly demand computation efficiencies well beyond what can be achieved through business as usual.

As information technology become pervasive in society and ubiquitous in our lives, the desire for always-on, always-available, embedded everywhere, and human-centric information systems may call for a different computation paradigm.

In this talk, I will describe the use of nanoscale electronic devices that emulate the functions of the biological synapse. The goal is to develop hardware technologies for brain-inspired computing and electronic emulation of the brain. Phase change memory is employed to demonstrate the spike-timing-dependent plasticity (STDP) behavior of the biological synapse. A small array of such devices are connected in a recurrent Hopfield network to perform pattern recognition tasks and the tradeoff between variation tolerance and the speed/energy performance of the network is studied. The use of metal oxide resistive switching memory (RRAM) presents another interesting possibility. The stochastic nature of the physics of resistive switching enables RRAM to serve as analog weights in a neural network. It is possible to tune the RRAM to introduce randomness for hyperdimensional computation for robust processing of perceptual data. I will describe on-going collaborative efforts to demonstrate in hardware, small and medium-scale system applications using electronic synapses integrated with CMOS neurons.

Biography:  
H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. At IBM, he held various positions from Research Staff Member to Manager, and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM’s strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. His present research covers a broad range of topics including carbon electronics, 2D layered materials, wireless implantable biosensors, directed self-assembly, nanoelectromechanical relays, device modeling, brain-inspired computing, and non-volatile memory devices such as phase change memory, conductive bridge memory, and metal oxide resistance change memory. He is a Fellow of the IEEE. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology in 2005 – 2006, sub-committee Chair of the ISSCC (2003 – 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems.

*** All are welcome to attend ***

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